Contact resistance in organic thin film transistors

Graciela B. Blanchet, C. R. Fincher, and Michael Lefenfeld DuPont, Central Research and Development, P.O. Box 80356, Wilmington, Delaware 19880-0356

J. A. Rogers

University of Illinois, Urbana-Champaign, Illinois 61801

(Received 14 August 2003; accepted 18 November 2003)

This letter reports on the unexpected dependence of contact resistance on the dielectric layer for pentacene thin film transistors with printed organic conducting electrodes. While the intrinsic mobility is weakly reliant on the dielectric, the contact resistance does vary considerably with dielectric layer. We show that while morphological changes are not apparent, contact resistances vary by an order of magnitude. This result suggests that the barrier to charge injection may depend not only on interactions at the complex triple interface but also on the details of the electronic structure at the semiconductor/dielectric interface. © 2004 American Institute of Physics. [DOI: 10.1063/1.1639937]

The performance of organic thin film transistors (TFT) has improved dramatically. While early on, the feasibility of organic electronic materials was illustrated by fabricating integrated circuits^{1,2} and active-matrix displays³ using photolithography, the more recent work explores using printing techniques. Fabrication approaches, such as soft lithography,⁴ thermal imaging,⁵ and ink jet,⁶ may enable commercialization of inexpensive, flexible electronic devices. Although much effort has focused on improving materials; the intrinsic electrical properties of the semiconductor as well as the gate dielectric and conducting electrodes. Geometrical factors such as channel length⁷ and interfacial properties at the contact⁸ that also critically determine TFT performance have not received much attention.

Our recent work⁹ demonstrated materials and patterning approaches for achieving both high-resolution electrodes and small contact resistances. We report the dependence of contact resistance on the chemical nature of the gate dielectric in a pentacene TFT. In these devices, pentacene was evaporated onto polyaniline/nanotube contacts printed via thermal transfer, a dry printing technique capable of patterning multiple layers of electronic materials over large areas ($\sim 1 \text{ m}^2$) with micron resolution (10 μ m). TFT performance relies not only on the ability to print short channel lengths but most critically on the low contact resistance of the electrodes to the semiconductor layers. The strong correlation between the contact resistance of our bottom contact printed DNNSA-PANI/SWNT electrodes and the dielectric was quite surprising. These results, in combination with the ability to print the electrodes with high resolution and speed are important features for the fabrication of low cost organic devices.

The devices were built on a flexible poly(ethylene terephthalate) substrates sputtered with 100 nm indium tin oxide for common gate electrodes. Polyhydroxystyrene (PHS) (Aldrich, 8000 MW) was rod coated onto the gate layer to a 1 μ m thickness and di-nonyl naphthalene sulfonic acid doped polyaniline/single wall nanotube composite (DNNSA–PANI/SWNT) source–drain electrodes printed on top. The details of the printing process have been previously described.^{5,10} The polyaniline composite electrodes, ~1 μ m

thick, have a conductivity of ~ 3 S cm. The TFT channel lengths, defined as the distance between source and drain were varied from 10 to 500 μ m, the channel width (W) was 1 mm. The transistors are completed by thermally evaporating 200 Å of pentacene through a shadow mask at 0.2 Å/s on top of the printed structures. Pentacene was evaporated, after an *in situ* purification step at 150 °C for 30 min at a base pressure of 3×10^{-8} Torr onto room temperature substrates.

To quantify the behavior of the contacts, we studied the channel length dependence of the device resistance at small source/drain voltages, where the effects of contacts should be most pronounced. A top view of the test structures used in these measurements is shown in Fig. 1(a). Although this type of bottom contact geometry enables the semiconductors to be deposited last, it is generally observed that it leads to either



FIG. 1. (a) Micrograph of thermal transfer printed patterns of DNNSA– PANI/SWNT source/drain electrodes; (b) current–voltage characteristics of organic transistors that use thermal transfer printed DNNSA–PANI/SWNT source/drain electrodes, ITO gates, glass resin gate dielectrics, and plastic substrates. The gate voltage varies from 0 to -100 V in steps of -20 V. The channel length and width are $100 \ \mu$ m and 1 mm, respectively. The inset shows the linear behavior of the device at small source–drain voltages in a bottom contact configuration. The characteristics of these devices are consistent with contacts that have ideal ohmic character; (c) current–voltage characteristics of transistors with printed DNNSA–PANI electrodes in a top contact configurations at small source–drain voltages.

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FIG. 2. Analysis of contact resistances and intrinsic channel mobilities from pentacene transistors with DNNSA-PANI/SWNT source/drain electrodes printed via thermal transfer. (a) Width-normalized channel resistance (R) as a function of channel length at gate voltages varying from -40 to -100 V at 20 V interval for phs (a) and glass resin (c). The transistor width in all cases is 1 mm. The contact resistance as a function of gate voltage for PHS and GR are shown in (b) and (d), respectively.

non-ohmic or highly resistive contacts compared to source/ drain electrodes deposited on top of the semiconductor (i.e., top contact geometry).^{11–15} Figure 1(b) shows the I-V characteristics of pentacene transistors that use electrode patterns similar to those shown in the inset. Source drain voltages (V_{sd}) ranged from 0 to -100 V and gate voltages (V_{g}) were varied from 0 to -100 V. The inset in Fig. 1(b) illustrates typical I-V characteristics at source/drain voltages (V_{SD}) that are smaller than the gate voltage (V_G) . The linear behavior is consistent with ideal ohmic contacts (or contacts whose effects on the device response are negligible). The contact resistance, R_c , was obtained from the L=0 intersection of the measured device resistance, R, as a function of channel length.¹⁶ R was obtained from the inverse slope of the linear I-V curves in the V_{sd} regime. The total resistance, R, can be related to a channel length dependent resistance, R_{ch} , and a channel length independent contact resistance, R_c , that is associated with the contacts, according to models developed for amorphous silicon top contact transistors. The current-voltage characteristics at low source/drain voltages shown in Fig. 1(c) show that devices with top contact printed PANI electrodes are slightly non-ohmic when compared to the bottom contact PANI counterpart.

Figure 2 shows a plot of RW as a function of channel length L at various gate voltages for PHS TFTs. This plot has information about both the intrinsic channel resistance (R_{ch}) and contact resistance (R_c) .^{15,16} R_c was determined from the y intercepts of linear fits to data at each V_{o} . The contact resistance as a function of gate voltage, extracted from the L=0 intersection, is shown in Fig. 2(b). Clearly, the gate voltage modulates the contact resistance. The results show that R_c decreases with increasing gate voltage reaching 12 $k\Omega$ at $V_g = -100$ V. The mobility and threshold voltages determined from a linear fit to the data were $0.31 \text{ cm}^2/\text{V} \text{ s}$ and 5.9 V. The calculated saturation, $\mu_{sat} = 0.32 \text{ cm}^2/\text{V} \text{ s}$, and intrinsic mobilities, $\mu_t = 0.34 \text{ cm}^2/\text{V}$ s from the pentacene has large grains as characteristics in high mobility thin films Downloaded 04 May 2004 to 128.174.209.28. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp



FIG. 3. (a) Scanning electron micrograph (SEM) of a 10 μ m channel with printed DNNSA-PANI/SWNT source and drains at the edge; (b) AFM of a region in the middle of the channel of a pentacene transistor that uses printed DNNSA-PANI/SWNT electrodes like those shown in (a); (c) SEM of the pentacene grains at the source/channel interface; (d) SEM of a Au electrode on pentacene.

devices all yielding similar results, to within experimental error. As we have previously reported,⁹ the effective mobilities of PHS devices with printed DNNSA-PANI electrodes is also larger than (\sim 1.5 times) those of similar devices that use top contact evaporated gold source/drain electrodes.

As shown in Figs. 2(a) and 2(c) the normalized resistance curves merge at a channel length value, L_{a} , which is independent of the gate voltage. L_{ρ} can be understood as additional channel length, introduced by the presence of the contacts. RW and R_c for TFTs with organosilesquioxane dielectric (GR) are shown in Figs. 2(c) and 2(d), respectively. As shown in Fig. 2, L_o varies both with the specific nature of the dielectric layer as well as with the contacts themselves. While L_{ρ} is ~0 for PHS, it reaches about 10 μ m for GR and 15 μ m for pentacene devices with top contact Au electrodes and a SiO₂ dielectric layer lead.¹⁵

The value of L_o , is extremely important for engineering devices for practical applications, since it defines the length at which further reductions in physical channel length yield only small or negligible increases in linear regime current output.

In order to investigate further the cause for the different L_{a} values, we examined by atomic force microscopy the morphology of 250 Å pentacene films evaporated onto printed DNNSA-PANI/SWNT electrodes and into the channel. These micrographs are shown in Figs. 3(a) and 3(b), respectively. In addition, scanning electron micrographs (SEM) of the triple interface formed at the DNNSA-PANI/ SWNT electrode edge, dielectric and pentacene and of top contact Au on evaporated pentacene are shown in Figs. 3(c) and 3(d), respectively.

The micrographs in Figs. 3(a) and 3(c) suggest that undisturbed crystal growth at the electrode interface, is not necessary to achieve ohmic contact. While printed DNNSA-PANI/SWNT electrodes are quite rough, showing irregular edges with pentacene not exhibiting the well-defined terraces in the characteristic thin film face, pentacene in the channel has large grains as characteristics in high mobility thin films [Fig. 3(b)]. As shown in Fig. 3(c), the widely different morphologies of the pentacene film on the electrode [Fig. 3(a)] and at into the channel [Fig. 3(b)] are effectively coupled nearby the electrode edge [Fig. 3(c)]. Pentacene very effectively weaves through the rough electrode edge, where a range of crystals of various sizes and orientations is observed, into the channel, achieving uniform grain size within 60 nm from the edge. It is interesting, however, that despite the disturbed crystal growth on the electrodes itself and at its edge, contacts are ohmic and show remarkably low contact resistance and good performance.

The efficient charge transport despite the various grain sizes and orientations at the contact suggests that morphology is not the only determining factor in the measured electrical properties. Perhaps the noted differences in the electrical characteristics may be associated with specific chemical interactions that are operative at the electrode/dielectric and dielectric/pentacene interfaces. These chemical interactions can influence how adjacent layers are formed and how "tightly" they interact with each other once in the device. The large differences in contact resistance observed between PHS and GR with micrographs reflecting essentially undistinguishable pentacene morphologies (in terms of grain size, shape, orientation, distribution, and extent of region of pentacene weaving) at the contacts perhaps suggests differences in charge injection at the dielectric and electrode surface. The interactions at the PANI/PHS interface are expected to be reasonably strong. PHS with an electron acceptor, the OH group can perhaps interact with PANI via H bonding, or act like an acid. In the former case, PANI becomes somewhat negative attracting the proton and PHS becoming somewhat positive drawing additional electron density into the PHS ring. Alternatively, PHS can give up a H and act like an acid, since both PANIs NH and N links are H bond acceptors. In contrast, the glass resin is basic in character. The initiator, an amine, is not fully removed when crosslinked and can withdraw electrons from the N and NH groups in the PANI. The effect of the basic or acidic nature of the dielectric on the Schottky barrier at the contacts and, thus, contact resistance is currently under investigation.

Although the pentacene/dielectric interface clearly has a weaker interaction, chemical differences of the dielectric layer influence pentacene growth and grain sizes. It has been shown that pentacene growth on SiO_2 with OH and H functionality show clear morphological differences. Thus, it is likely that pentacene growth on PHS with OH groups and GR with H groups may similarly influence pentacene growth.

In summary, this letter reports on unexpected dependence of contact resistance on the dielectric layer. While the intrinsic mobility is weakly reliant on the dielectric, the contact resistance does vary considerably with dielectric layer. While the morphology of pentacene evaporated onto PHS and GR at the contact and into the channel are nearly undistinguishable their contact resistances vary by $10 \times$. This result suggests that the barriers to charge injection may depend not only on interactions at the complex triple interface but also at the dielectric/electrode and/or semiconductor/ dielectric interfaces. Our results show that while the contact resistance effectively adds 10 μ m in channel length for a GR dielectric, basic in nature, the effective channel length remains unchanged for PHS, a dielectric acidic in nature. These results suggest that understanding the chemical interaction at the organic dielectric electrode interface and, more specifically, the Schottky barrier at the contacts is necessary in order to minimize the contact resistance optimizing device performance. These fundamental issues are the focuses of our current work.

The authors would like to thank Dr. Gary Jaycox for stimulating discussions and his careful reading of the manuscript. We are grateful to Kevin Bailey for his able technical assistance in the preparation of the films.

- ¹G. H. Gelinck, T. C. Genus, and D. M. Leeuw, Appl. Phys. Lett. **77**, 1487 (2000); B. K. Crone, A. Dadabalapur, R. Sarperhkar, R. W. Filas, Y. Y. Lin, and Z. Bao (unpublished).
- ²J. H. O'Neil, W. Li, and H. Katz, J. Appl. Phys. 89, 5125 (2001).
- ³C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl, and J. West, Appl. Phys. Lett. **80**, 1088 (2002).
- ⁴J. A. Rogers, Z. Bao, K. Baldwin, A. Dodabalapur, B. Crone, V. R. Raju, V. Kuck, H. Katz, K. Amundson, J. Ewing, and P. Drzaic, Proc. Natl. Acad. Sci. U.S.A. **98**, 4835 (2001).
- ⁵G. B. Blanchet, Appl. Phys. Lett. 82, 1290 (2003).
- ⁶H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and P. Woo, Science **290**, 2123 (2000).
- ⁷H. H. Busta, J. E. Pogemiller, R. W. Standley, and K. D. Mackenzie, IEEE Trans. Electron Devices **26**, 2883 (1989).
- ⁸H. F. Bare and G. W. Neudeck, IEEE Electron Device Lett. 7, 431 (1986).
- ⁹M. Lefenfeld, G. B. Blanchet, and J. A. Rogers, Adv. Mater. (Weinheim, Ger.) **15**, 1188 (2003).
- ¹⁰G. B. Blanchet, Y. L. Loo, J. A. Rogers, F. Gao, and C. R. Fincher, Appl. Phys. Lett. **82**, 463 (2003).
- ¹¹J. A. Rogers, Z. Bao, K. Baldwin, A. Dodabalapur, B. Crone, V. R. Raju, V. Kuck, H. E. Katz, K. Amundson, J. Ewing, and P. Drzaic, Proc. Natl. Acad. Sci. U.S.A. **98**, 4835 (2001).
- ¹²Z. Bao, V. Kuck, J. A. Rogers, and M. A. Paczkowski, Adv. Funct. Mater. 12, 526 (2002).
- ¹³I. Kymissis, D. C. Dimitrakopoulos, and S. Purushothaman, IEEE Trans. Electron Devices 48, 1060 (2001).
- ¹⁴R. A. Street and A. Salleo, Appl. Phys. Lett. **81**, 2887 (2002).
- ¹⁵P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson, Solid-State Electron. **47**, 259 (2003); H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, and T. N. Jackson, *ibid.* **47**, 297 (2003).
- ¹⁶S. Luan and G. W. Neudeck, J. Appl. Phys. 72, 766 (1992).