Printing Techniques for Plastic Electronics*

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This article summarizes two recently developed patterning techniques for plastic electronics: microcontact printing and thermal transfer printing. It reviews the methods and their capabilities, and presents new results on their use in forming transistors and circuits with a range of organic semiconductors. Active matrix backplane circuits for large, mechanical flexible sheets of electronic paper and other display devices represent one class of realistic application whose patterning requirements can be satisfied with current versions of these printing approaches.

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Introduction

The most widely used techniques for micro and nanofabrication—photolithography, electron beam lithography and related methods—are spectacularly well suited to the types of applications in microelectronics and display systems for which they were principally designed. There are considerable challenges, however, in adapting these techniques to new applications in fields such as plastic and molecular electronics. In these cases, the complexity, the high capital and operating costs, the difficulty in patterning large areas, and the limited range of materials that can be directly patterned all represent significant disadvantages. In addition, the chemicals that are required for these methods—the resists, etchants, developers, solvents, etc., are incompatible with many interesting organic electronic materials. As a result, there is growing interest in new patterning techniques that avoid these limitations and can be used for plastic circuits. This emerging area of electronics is attractive because, when implemented with appropriate patterning techniques, it provides a route to devices that are formed at low cost, over large areas, on flexible plastic sheets, by low temperature solution casting, evaporating and/or printing.

Transistors are essential elements of these circuits. Figure 1 shows cross sectional views of two common geometries. Both use a semiconducting layer that is electrically connected to source and drain electrodes. A thin insulating film, i.e. the gate dielectric, isolates these electrodes and the semiconductor from an underlying gate electrode. The electrodes can be deposited on top of the semiconductor (top contact; Fig. 1a), or the semiconductor can be deposited on top of them (bottom contact; Fig. 1b). The region between the source/drain electrodes is known as the channel of the transistor. The separation between these electrodes defines the channel length, L; their lengths define the channel width, W.

In an accumulation mode device, the channel has a high effective resistance when no voltage is applied to the gate: the transistor is in its "off" state. When a voltage is applied to the gate, charges can be induced in the semiconducting layer at its interface with the gate dielectric. In this situation, current flows between the source and drain electrodes when there is a potential difference between them: the transistor is in its "on" state. The magnitudes of these "on" and "off" currents and the time required to switch between these two states determine, in part, the utility of a transistor in a circuit. The transistor must produce enough "on" current to activate or switch another part of a circuit or device, e.g., a pixel in a display, but it must not generate "off" currents that are large enough to cause unwanted switching. These key characteristics are governed by the mobility of the semiconductor, the efficiency with which it is coupled to the source/drain electrodes, i.e. the resistances associated with the contacts, the capacitance of the gate dielectric, and the ratio of the channel width to its length.

Reducing the channel length increases the 'on' currents. The ability to print the source/drain electrodes at high resolution is therefore crucial to achieving good performance. Just as shrinking the channel lengths in silicon transistors provides a driving force for progress in conventional microelectronics, this same strategy can be important for increasing the performance of plastic electronics. For many envisioned applications in dis-

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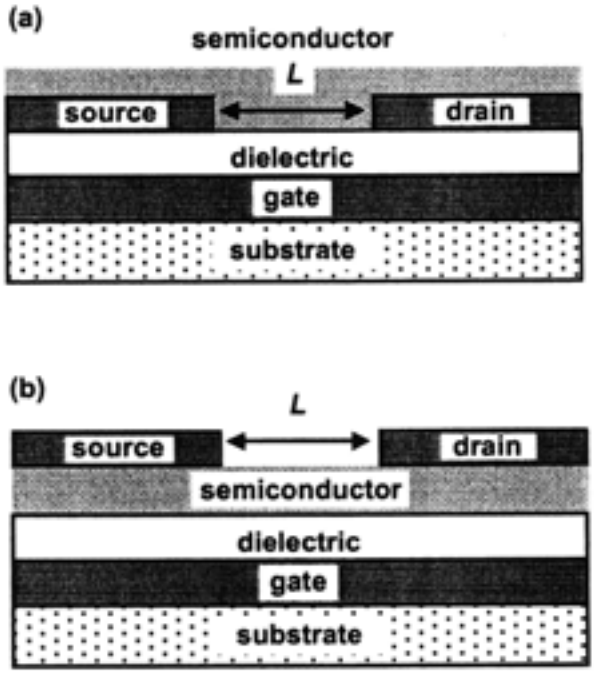

Figure 1. Schematic illustrations of two device geometries for organic thin film transistors. Part (a) shows the layout of a 'top contact' device in which the source and drain electrodes are deposited on top of the semiconductor. Part (b) shows the 'bottom contact' geometry in which the semiconductor is deposited on top of the electrodes. The separation between the electrodes defines the channel length, *L*.

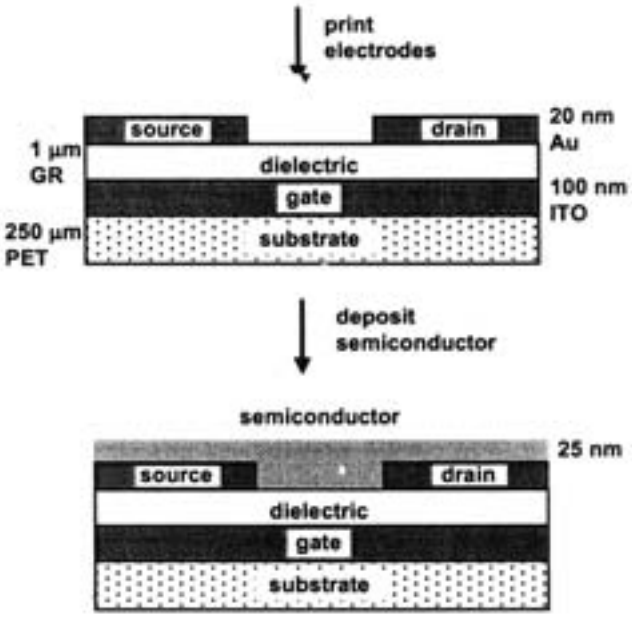

Figure 2. Sequence for fabricating 'bottom contact' organic transistors with printed metal source/drain electrodes. Microcontact printing patterns the electrodes from a uniform layer of metal of Au/Ti deposited on a substrate (poly(ethylene terephthalate) – PET) that supports a gate electrode (indium tin oxide – ITO) and a thin dielectric layer (glass resin – GR). Depositing the semiconductor film on top of the electrodes completes the transistor.

plays and other systems, the ability to print with better than ~25–50 μm resolution rapidly and over large areas begins to enable basic devices that have some commercially significant applications.

Several techniques have been demonstrated for this patterning task, including a type of photolithographic processes that relies on the photochemical conversion of polymers from non-conducting to conducting states,[1,2] specialized adaptations of ink jet[3] and screen printing,[4,5] certain types of molding[6] and imprinting[7] techniques and a nanotransfer printing method.[8–10] Here we describe two approaches which we believe are particularly promising: one based on a high resolution form of rubber stamping[11–13] and the other on thermal transfer.[14] Both have already been demonstrated for relatively sophisticated plastic electronic systems.

Experimental

Figures 2 and 3 show two different means for using microcontact printing (μCP) in plastic electronics. Similar approaches can be used with a related technique known as nanotransfer printing. μCP uses high resolution rubber stamps and 'inks', e.g., alkanethiols, that form self assembled monolayers on the surface (thin gold film) that is printed.[11] These monolayers can act as resists for etching the unprinted areas. In Fig. 2, μCP defines 'bottom contact' electrodes directly on a substrate that supports a gate dielectric and a gate. Depositing an organic semicondutor on top of this structure yields a transistor. Figure 3 shows a different strategy which uses the same printing approach to produce 'top contact' transistors. Here, electrodes are patterned and

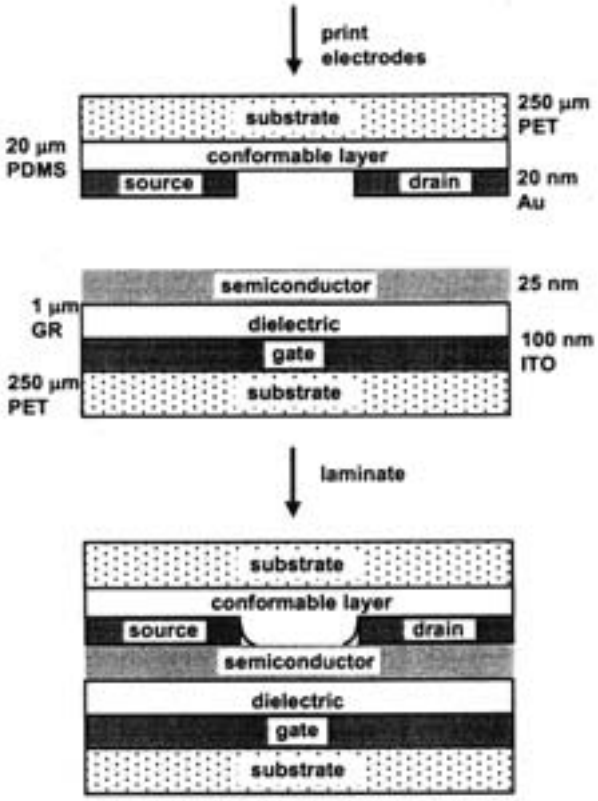

Figure 3. Sequence for fabricating 'top contact' organic transistors with printed metal source/drain electrodes. Microcontact printing patterns electrodes of Au/Ti on a thin conformable layer (poly(dimethylsiloxane) - PDMS) on a plastic sheet (poly(ethylene terephthalate) - PET). Soft contact lamination of this sheet against a substrate that supports the semiconductor, gate dielectric (glass resin – GR), gate (indium tin oxide – ITO) completes the transistor.

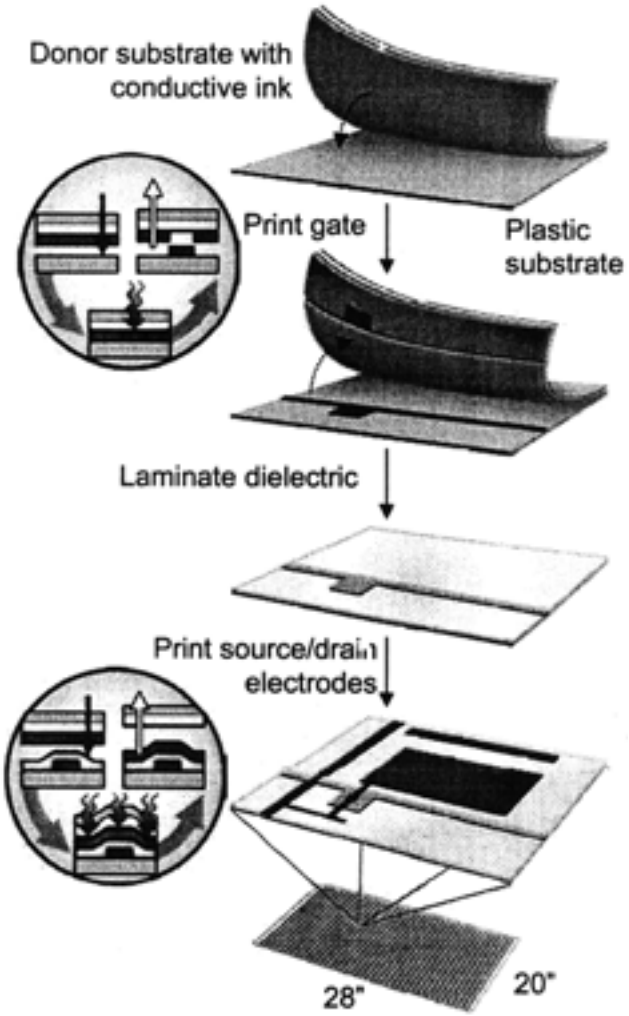

Figure 4. Sequence for patterning arrays of interconnected transistors using thermal transfer printing. A donor sheet that is coated with a layer of conducting polymer is placed against the circuit substrate. The inset shows the process by which local heating with a laser causes the transfer of some part of the conducting polymer from the donor. Repeating these lamination, transfer printing, removing steps (shown in the circle insets on the left) allows purely additive, dry multilayer patterning of the type that is attractive for plastic electronics.

processed on a separate substrate that supports a thin conformable layer, e.g., ~20 μm thick layer of poly(dimethylsiloxane) formed by spin casting. These electrodes can be patterned by μCP or by other high resolution printing methods. Soft contact lamination of this structure against a substrate that provides the semiconductor, gate dielectric and gate yields a top contact transistor that is embedded between two plastic sheets.[8,15] For the work described here, μCP is performed with 'inks' of hexadecanethiol (~1 mM in ethanol) on gold (20 nm) × over titanium (1.5 nm; adhesion promoter) deposited using electron beam evaporation. Glass resin (GR) films spin cast to thicknesses of ~1 μm serve as gate dielectrics.[13,16] The substrate consists of a 250 μm thick sheet of poly(ethylene terephthalate) (PET) with a thin (100 nm) coating of indium tin oxide (ITO) for the gate.[13]

Figure 4 shows the second approach, known as thermal transfer printing, in which patterning proceeds via the purely additive, selective transfer of a solid film. This type of dry printing removes the challenging solvent compatibility requirements of multilayer circuits and expands considerably the range of usable materials. In addition, thermal printing maintains features desirable in large scale manufacturing such as high speed, resolution and registration. Figure 4 illustrates the process sequence for building a large area circuit. A donor film that is coated with a thin conducting layer to be patterned is placed against the receiver, i.e. circuit substrate, and selectively exposed to a laser beam. The heat generated by the absorption of the focused laser at the light sensitive layer in the donor partially vaporizes organics at the interface, thus propelling the exposed area of the conducting layer onto the receiver film. Lines and other patterns are printed by selectively exposing and transferring 5 μm × 2 μm pixels of the conducting layer onto the receiver. Since the beam is fully addressable, any pattern can be formed. After the printing of the gate layer, the next donor whose top layer has a different functionality, i.e. dielectric, is positioned and exposed. Multilayer electronic circuitry can be built in this fashion. Although a variety of conductors are compatible with this approach, we focus on a polymer system that consists dinonylnaphthalenesulfonic acid doped polyaniline (DNNSA-PANI) mixed with several weight percent of single wall carbon nanotubes (SWNT).

For structures formed using each of these fabrication approaches, the semiconductors were deposited onto unheated substrates by thermal evaporation through shadow masks at rates of 0.05–0.1 nm/s to thicknesses of ~25 nm. For the fluorinated copper phthalocyanine (FCuPc), the substrate was heated to ~100 C during the evaporation. The materials were obtained commercially and were used without further purification.

Results and Discussion

Microcontact Printing

Figure 5 shows some representative examples of structures patterned by μCP. The electrodes are formed on glass resin (~1 μm thick)/ITO (100 nm thick)/PET (250 μm thick) substrates, as indicated in Figs. 2 and 3. The top frame shows a test structure for a display circuit. The transparent ITO gate electrode is faintly visible as a line on the left part of the image. The source/drain electrodes and interconnects are printed in Au; they appear dark in this image. The transistor is in the middle left. The source/drain electrodes and the leads that connect to them consist of wires 10 μm wide. The resulting low overlap capacitance allows switching times of ~1 ms. The channel length in this case is also 10 μm, and the width is ~200 μm. The image at the bottom illustrates the level of registration that is possible with microcontact printing, even without implementing sophisticated staging apparatus or specialized stamps. These images were collected from the corners of a pattern that was printed in a single impression over an area of approximately 16 cm × 16 cm. The alignment of the source/drain electrodes (pairs of narrow vertical lines) are to within ~50 μm of the desired position in the middle of the gate electrode (gray vertical lines, patterned by shadow masking).[13]

Depositing semiconductors onto these structures yields transistors. One way to quantify the behavior of the resulting devices is to examine the behavior of the "on" current (I_{sd}) measured in a regime where the source/

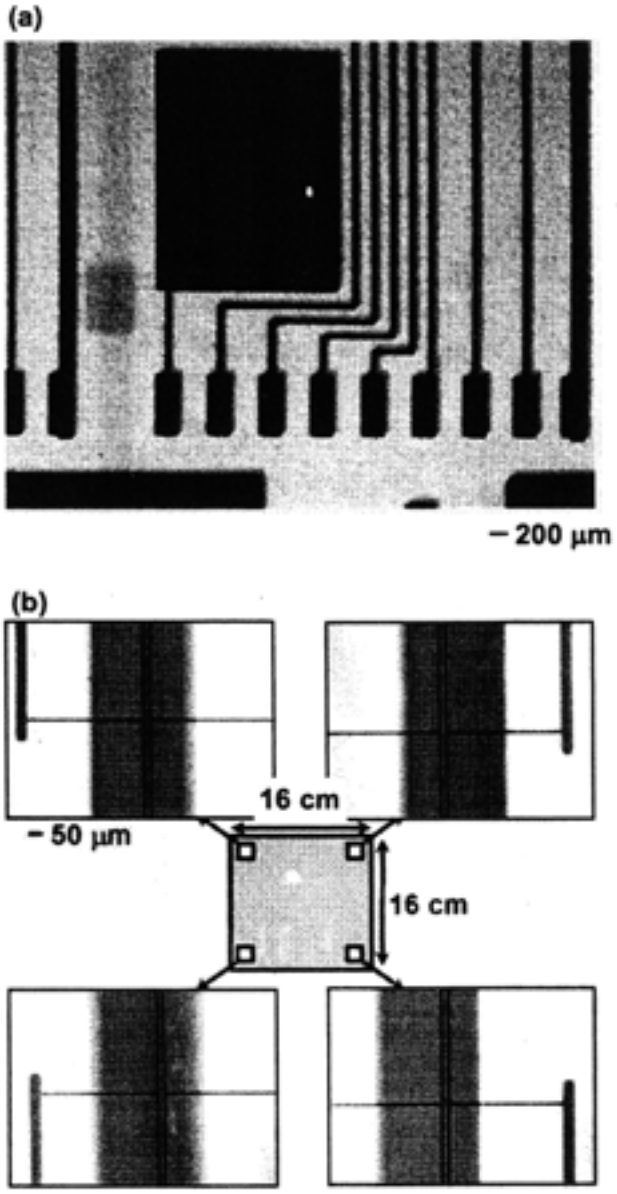

Figure 5. Optical micrographs of microcontact printed patterns of Au/Ti for the source/drain level of simple plastic circuits. Part (a) shows a test structure for a display circuit. The transistor is visible in the middle left. Part (b) shows the alignment of source/drain electrodes to an underlying gate (patterned by shadow masking) at four corners of a large printed area. The level of registration illustrated here (~50 μm) can be achieved even without the use of sophisticated staging systems or specially designed stamps.

drain voltage is larger than the gate voltage. Here the current, known as the saturation current, is independent of the source/drain voltage; it can be related to other characteristics of the device according to:[17]

$$I_{sd} = \frac{W}{2L} C\mu\left(V_g - V_T\right)^2 \quad (1)$$

where μ is the effective mobility of the semiconductor and C is the capacitance of the gate dielectric. V_g is the gate voltage and V_T is known as the threshold voltage. Transistors that have large "on" currents possess some combination of large μ, high ε, or high C. Limits on the overall physical size of a transistor for a particular application typically place an upper bound on W. The key properties therefore reduce to μ, C, and L. The patterning techniques, which are the focus of this paper, determine L.

Figure 6 shows some current-voltage measurements from transistors that use structures similar to those illustrated in Figure 5. The top frame corresponds to data collected from a p-channel transistor that uses the semiconductor dihexyl quinquethiophene (DH-α-5T),[18] printed source/drain electrodes of silver (~50 nm) deposited from an electroless plating bath[19] and a glass resin/ITO/PET substrate in the layout illustrated in Fig. 2. The gate voltage varies from 0 V to –75 V in steps of –15 V. The middle frame shows the characteristics of a similar device that uses the p-type organic semiconductor pentacene[20] with printed electrodes of Au (20 nm) / Ti (1.5 nm) and the same gate, gate dielectric and substrate combination. The gate voltage varies from 0 V to –50 V in steps of –10 V. The bottom frame shows measurements from a device that uses copper pthalocyanine (CuPc)[21] with source/drain electrodes of Au (20 nm) formed by microcontact printing on top of the semiconductor/gate dielectric/gate stack. The gate voltage varies from 0 to –100 V in steps of –20 V. The mobilities computed from these data using Eq. (1) correspond well to the range of values that are observed with test structures formed on the same types of substrates by shadow evaporating contacts on top of the semiconductor: 0.05 for DH-α-5T, 0.1 for pentacene and 0.002 for CuPc (all cm^2/ V s). It is noteworthy that the effective mobility observed in the printed top contact CuPc device is similar to that measured in devices with bottom contact printed electrodes, in spite of the fact that in a top contact device, the semiconductor itself is exposed to the etching solution used in microcontact printing.

Thermal Transfer Printing

Figure 7 shows some typical structures formed by thermal transfer printing. Part (a) shows a top view optical micrograph of a multilayer structure in the geometry of a active matrix drive circuit for an element of a display.[13,14] The source, drain, gates, and interconnects were printed with DNNSA-PANI/SWNT and the dielectric was a 1 μm methacrylate co-polymer layer laminated onto the gate at 120°C using a standard Waterproof® laminator. Figure 7b illustrates a printed, 20 μm wide DNNSA-PANI/SWNT source line. This image reveals SWNT ropes anchored at the line edge and extending into the channel, which suggests that printed pixels may carry ropes that extend beyond their volume. Portions of a rope lying outside the pixel being transferred become pulled out and exposed if the neighboring pixel is not transferred. A detailed view of a single tube extending into the channel is shown in Fig. 7c. It is possible that these tubes enhance the electrical contact between these conducting lines and layers of organic semiconductors that are deposited on top. Micrographs of pentacene grains on the DNNSA-PANI/SWNT structures, near the dielectric/electrode interface and on the dielectric in the middle of the transistor channel show an absence of any disruptions in grain growth that could potentially be associated with the SWNT's.

Although it is possible that metallic SWNT's extending into the channel could modulate the transistor current, such effects were not observable in the range of

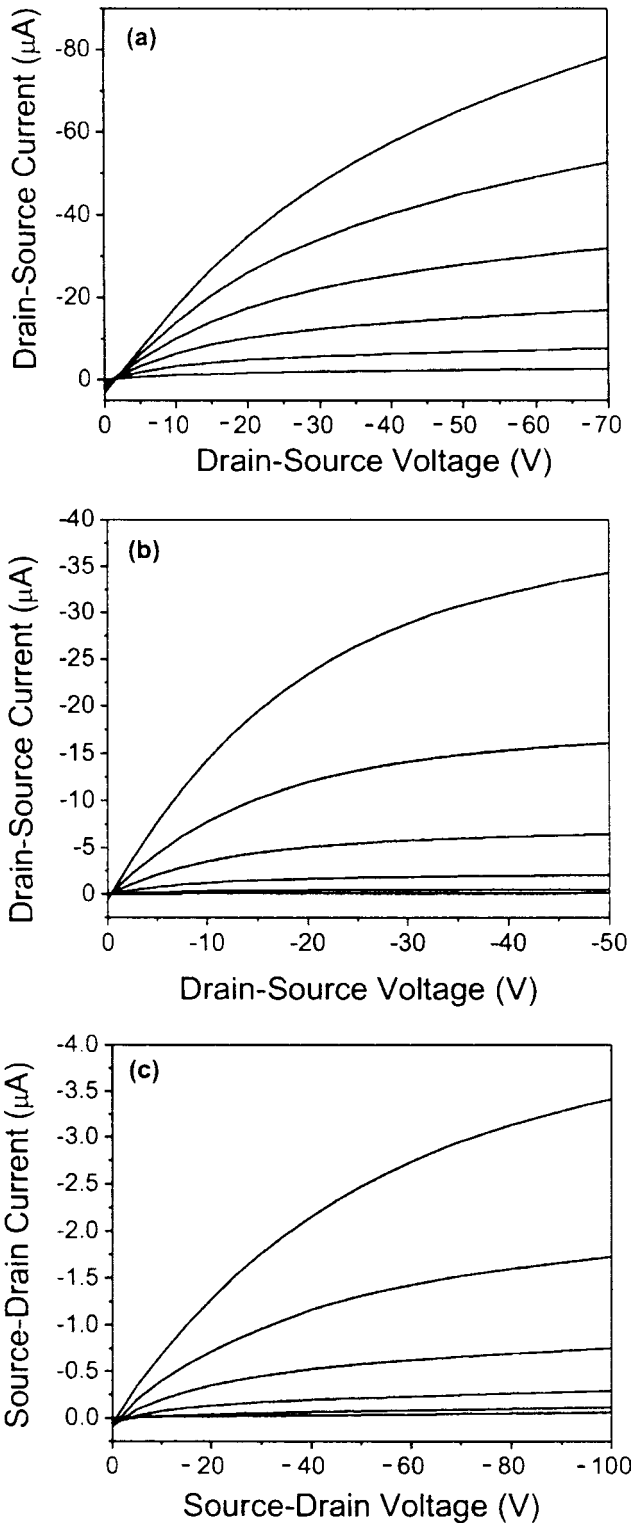

Figure 6. Current-voltage characteristics for organic transistors that use source/drain electrodes defined by microcontact printing. Data in parts (a), (b) and (c) use the semiconductors dihexylquinquethiophene, pentacene and copper pthalocyanine respectively. The device in part (c) uses source/drain electrodes patterned by microcontact printing and etching a layer of uniform metal (Au) deposited on top of the copper pthalocyanine. The other two devices use printed bottom contact electrodes of Au/Ti.

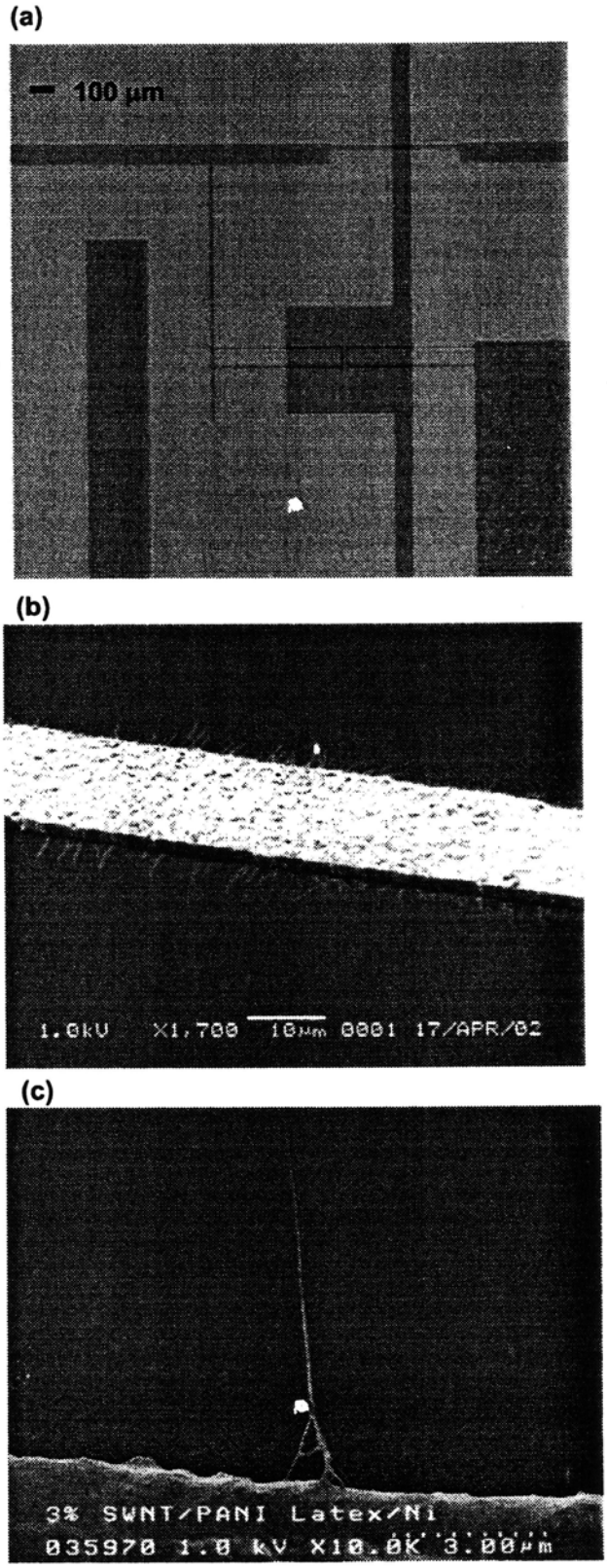

Figure 7. Part (a) shows a transistor in an active matrix display circuit formed by thermal transfer printing. The gate, source, drain and interconnects were all printed with DNSSA-PANI/SWNT. The scanning electron micrograph (SEM) in part (b) shows a transferred PANI/SWNT 20 μm line. Numerous SWNT's anchored onto the edge of the conducting line and extending into the channel are also visible. The SEM in part (c) shows a single SWNT rope extending from the PANI/SWNT source line into the channel.

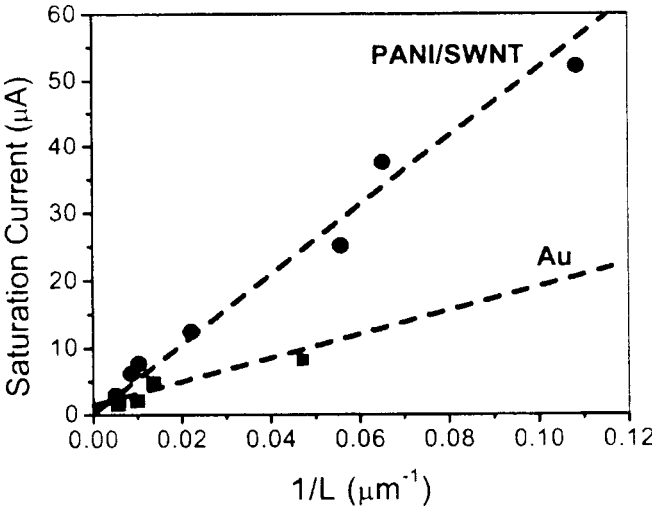

Figure 8. Source-drain current at source-drain voltages of –100 V at gate voltages of –100 V as a function of the inverse channel length (L) for pentacene transistors that use source drain electrodes printed with DNSSA-PANI/SWNT via thermal transfer. The data show the expected linear scaling of current with $1/L$. Also shown are data collected from devices that use gold source/drain electrodes deposited on top of the semiconductor (solid squares). The dashed lines are guides to the eye.

channel geometries that we investigated. For example, Fig. 8 shows the 'on' current at source/drain voltages of –100 V as a function of $1/L$ at maximum gate voltage (–100V) for sets of transistors with 15 μm wide source and drain electrodes, 750 μm channel width, and channel lengths ranging from 10 to 250 μm. As expected, the maximum 'on' currents scale linearly with $1/L$ for a given array of transistors.[14] The absence of deviations from linearity at small channel lengths is consistent with good electrical contacts and negligible adverse effects of the SWNT's that protrude into the channel region. This figure also compares currents measured using devices with source/drain electrodes evaporated on top of the semiconductor. The enhanced performance observed in the thermal transfer printed devices is described in more detail below.

Figure 9 shows typical current-voltage measurements from pentacene, sexithiophene (α-6T),[22] FcuPc,[23] and quaterthiophene (α-4T)[24] transistors with source and drains printed via thermal transfer. The transistors have a structure similar to the microcontact printed ones described in Fig. 2: glass resin (~1 μm)/ITO (100 nm)/PET (250 μm). Source and drain electrodes of DNNSA-PANI/SWNT were printed onto this substrate by thermal transfer. The channel width in all cases is 750 μm. The conductivity of the transferred 1 μm thick DNNSA-PANI/SWNT film was about 3 S/cm. The top frame corresponds to data collected from a p-channel transistor that uses the semiconductor pentacene, with a channel length of 22 μm, as indicated in the inset. The gate voltage was varied from 0 to –100 V in –20 V steps. The second frame shows the characteristics of a similar device that uses the p-type organic semiconductor α-4T and has a channel length of 17 μm. The third frame shows measurements from a device that uses the n-type semiconductor FCuPc. The gate voltage varies from 0 to 100 V in steps of 20 V and the channel length was 22 μm. The bottom frame shows measurements from a device that uses α-6T with a channel length of 24 μm.

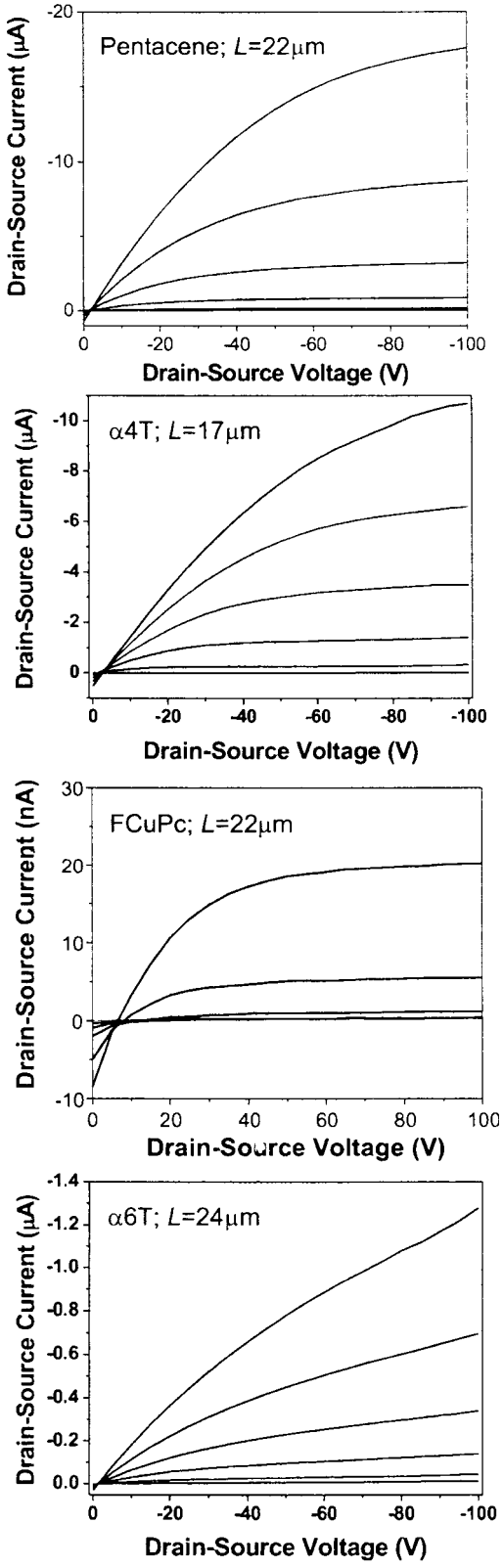

Figure 9. Electrical characteristics of transistors with source and drains printed via thermal transfer with DNNSA-PANI/SWNT. The devices use an ITO gate, a glass resin dielectric with printed source and drain electrodes (750 μm channel width; channel lengths indicated in the insets). The organic semiconductors include evaporated pentacene (a), quaterthiophene (α-4T) (b), fluorinated copper pthalocyanine (FCuPc) (c) and sexithiophene (α-6T) (d). In all cases, except for the FCuPc device, the gate voltages vary from 0 to –100 V, in –20 V steps. For FCuPc, the gate voltage varies from 0 to 100 V in 20 V steps.

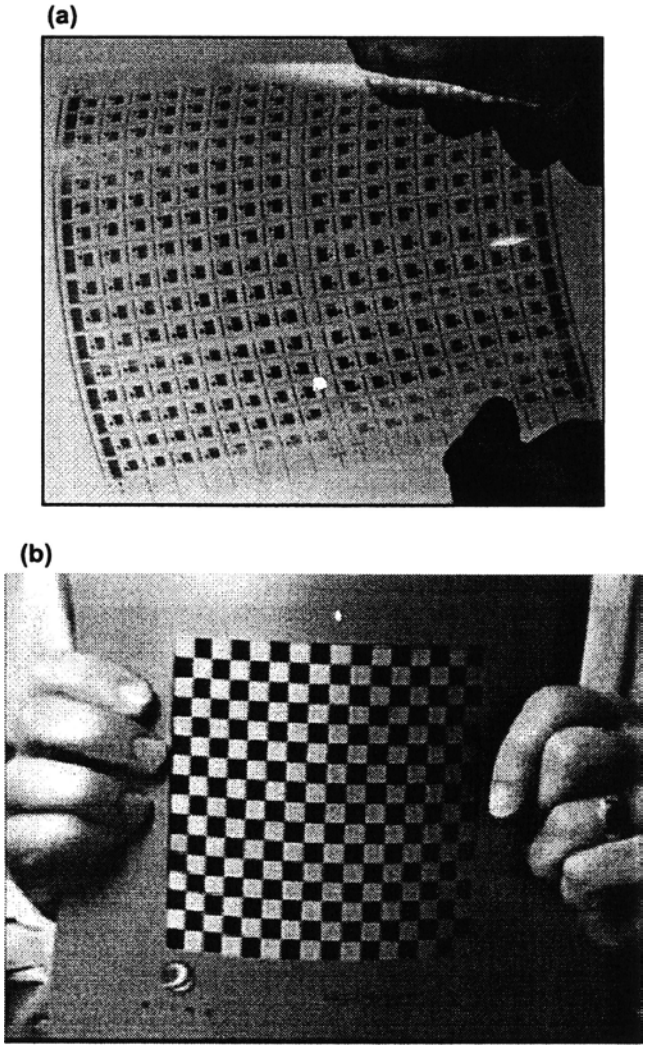

Figure 10. Part (a) shows an image of a flexible plastic active matrix backplane circuit whose finest features were defined by microcontact printing. Part (b) shows a flexible paperlike display that uses a circuit similar to the one shown in (a).

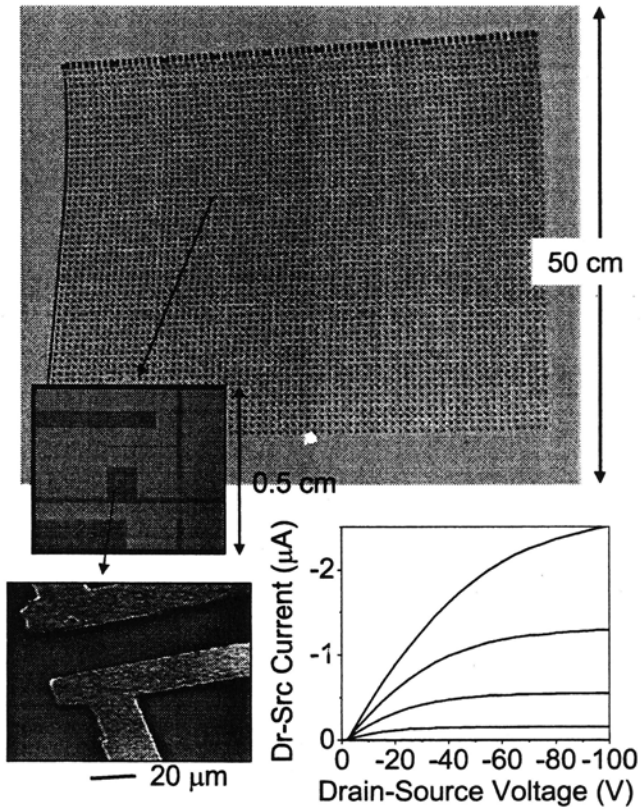

Figure 11. Active matrix backplane circuit formed by thermal transfer. A photograph of a 50cm × 75 cm printed panel is shown on the top. The micrograph at the middle left illustrates a single printed transistor and the detail of the source and drain electrodes in the location of a single pixel. The scanning electron micrograph on the bottom left provides a high resolution view of the source/drain electrodes and the channel region. The graph on the bottom right shows the electrical characteristic of one of the transistors in the large printed panel. The gate voltage varies from 0 to –100V in –20V steps.

The effective mobility of the printed devices, computed from the saturation current at high voltage using Eq. (1) was 0.27 cm^2/Vs for pentacene, 0.07 and 0.0014 cm^2/Vs for α-4T and α-6T, respectively and 0.002 for FCuPc. The mobilities of control devices with Au source and drain evaporated on top of the semiconductor and patterned using shadow masks to define similar W/L ranged from values that were comparable to those of the DNNSA-PANI/SWNT devices (for FCuPc) to values between 1.5 to several times lower (for the other semiconductors). A comparison of currents in pentacene devices is shown in Fig. 8. The threshold voltages and 'off' currents in all cases are similar, to within expected device-to-device variations. The good electrical performance of the thermal transfer printed devices derives, in part, from the low contact resistance between the DNNSA-PANI/SWNT source/drain electrodes and the organic semiconductors. Recent measurements quantify the ohmic behavior of these contacts and provide some morphological evidence for their low resistance. The differences in apparent mobility reflect differences in contact resistance between the organic/semiconductor and metal/semiconductor interfaces.

Not only can these printing techniques form individual transistors with good characteristics, but they can also be used for large area circuits that have performance sufficient for interesting systems that might have commercial value. Figure 10 shows images of a 6" × 6" plastic active matrix backplane circuit formed by microcontact printing using the materials and procedures described previously.[13] Pentacene serves as the semiconductor in this case. Laminating this circuit against an unpatterned layer of a microencapsulated electrophoretic ink yields an electronic paper-like display.[13,25] See the bottom frame of Fig. 10. The details of this device can be found elsewhere.[13] Although the number and size of the pixels are not suitable for realistic applications, there are no inherent limitations in the printing techniques which prevent more pixels and higher resolution.

Figure 11 shows a picture of a backplane with a similar layout, but much larger in size. This circuit was formed using thermal transfer printing and lamination

for all of the layers of the circuit according to the procedures illustrated in Fig. 4 followed by pentacene evaporation.[14] First a PANI/SWNT donor and a flexible receiver are positioned and held in contact by vacuum. Gates were then printed by selectively transferring DNNSA-PANI/SWNT from a donor film onto a flexible receiver as previously described. The receiver was then removed for the lamination of a 1 μm methacrylate copolymer layer over the whole area and re-positioned in registry for the printing of the source and drain layer. The backplane was completed by evaporation of unpurified pentacene through a shadow mask. Although the printing system maintains a 2 to 5 μm registration when imaging via the transfer of sequential layers onto a fixed receiver, it lacks built-in registration once the receiver is removed. Registration was achieved by aligning the receiver onto preset orthogonal edges on a carrier sheet that could, in turn, be precisely located onto the drum of the printer. Even with this rudimentary approach, it was possible to achieve registration errors of less than 200 μm over the 4000 cm^2 area. The circuit contains 5000 transistors with 20 μm channels printed onto a 50 cm × 80 cm flexible substrate. Micrographs of a typical transistor are shown in the lower left hand corner of Fig. 11, and the transfer characteristics of a typical transistor in the panel are shown in the lower right.

Conclusions

This article summarizes some of our recent work in the area of printing techniques and plastic electronics. It also presents new data from printed transistors that use several different organic semiconductors in a variety of device geometries. In all cases, we observed good performance. Microcontact printing for the source/drain electrodes is attractive because it provides a simple and potentially low cost route to high resolution, i.e. small channel lengths, L, structures that can be used to build transistors which produce large 'on' currents even with the moderate to low mobilities that are available from currently known organic semiconductors. It is also compatible with solution deposited metals, i.e. electroless silver.[19] It is conceivable that the technique could be used easily for manufacturing in high volumes and large sizes, insofar as it employs elastomeric materials of similar thickness and modulus to those used in standard flexography on conventional printing presses operating in reel-to-reel configurations.[12] Its main disadvantage is that it is compatible only with a narrow set of materials. The most well developed forms of microcontact printing use thiol inks, thin films of coinage metals and wet etching. Additional work will be required to invent methods for using this type of printing to pattern dielectric and semiconductor layers with similar resolution. Techniques based on selective dewetting from printed hydrophilic/hydrophobic patterns may be promising.[26,27]

Although the thermal transfer printing technique does not offer resolution as high as microcontact printing, it does have enormous flexibility in the materials that can be patterned. It also benefits from its all 'dry' and purely additive operation; it does not require etchants or solution routes for depositing or patterning the key materials. It is necessary, however, to balance the adhesion between the layers that are sequentially transfer such that interfaces have intimate physical and electrical contact. In addition, current commercial systems have pixel sizes of 5 × 2.2 μm, which limit the resolution. With the current DNSSA-PANI/SWNT formulation and a printer of this type, it is possible to print 10 μm channels and 25 μm lines. For applications that demand sub 20 μm resolution, it may be possible to combine microcontact and thermal transfer printing: high resolution source/drain electrodes printed with μCP could be used with other components that are patterned by thermal transfer. These and other strategies that combine and match different patterning techniques may provide an attractive means for building plastic circuits.

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