Contact resistance in organic transistors that use source and drain electrodes formed by soft contact lamination

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(Received 15 January 2003; accepted 25 February 2003)

Soft contact lamination of source/drain electrodes supported by gold-coated high-resolution rubber stamps against organic semiconductor films can yield high-performance organic transistors. This article presents a detailed study of the electrical properties of these devices, with an emphasis on the nature of the laminated contacts with the *p*- and *n*-type semiconductors pentacene and copper hexadecafluorophthalocyanine, respectively. The analysis uses models developed for characterizing amorphous silicon transistors. The results demonstrate that the parasitic resistances related to the laminated contacts and their coupling to the transistor channel are considerably lower than those associated with conventional contacts formed by evaporation of gold electrodes directly on top of the organic semiconductors. These and other attractive features of transistors built by soft contact lamination suggest that they may be important for basic and applied studies in plastic electronics and nanoelectronic systems based on unconventional materials. © *2003 American Institute of Physics.*
[DOI: 10.1063/1.1568157]

I. INTRODUCTION

The field of plastic electronics is interesting partly because it has the potential to enable useful devices — flexible paperlike displays, woven electrotextiles, low-cost identification tags, etc. — that might be difficult to achieve with established silicon technologies. Progress in plastic electronics is driven mainly by improvements in the mobilities of organic semiconductors, increases in the capacitance of suitable gate dielectrics, and reductions in key dimensions of the devices. Size reduction, in particular, represents a powerful approach that has proven to be invaluable for progress in silicon microelectronics. Decreasing transistor channel lengths, for example, increases their current output capability and their switching speed. For organic semiconductors, which have typical grain sizes in the 100–500 nm range, submicron channels also have the potential to increase the effective mobilities by decreasing the number of grain boundaries in the channel or by avoiding them altogether. Recent efforts to enhance the mobility[1] as well as to reduce the size[2–5] of organic thin film transistors have raised interesting questions about fundamental limits. The contact resistance between the source/drain electrodes and the semiconductor becomes increasingly important to device performance as the channel length decreases. In fact, when the channel length is small enough that the contact resistance dominates the overall device resistance, there is limited practical benefit to reducing this dimension further. Understanding the electrical properties of the contacts and their dependence on electrode materials, organic semiconductors, and processing conditions is therefore clearly important from this engineering perspective. It is also crucial for interpreting measuréments from short channel devices designed for basic study of nanoscale charge transport in organics.

When used with most organic semiconductors, bottom contact metal source/drain electrodes (i.e., semiconductor deposited on top of the electrodes) that are patterned by conventional or unconventional approaches often yield transistors that exhibit poor characteristics such as highly nonohmic behavior in the linear regime or low-effective mobility, or both. Disturbed crystal growth in the semiconductor film at the triple interface formed by the dielectric, metal, and semiconductor appears to be partly responsible for this poor performance. Chemically treating the electrodes can avoid some of these problems.[6] Bottom contact devices with microcontact printed electrodes can show ohmic behavior and good mobilities, but only when the devices are thermally annealed and when other steps in the processing are carefully controlled and optimized.[7] Organic transistors based on top or bottom contact source/drain electrodes of conducting polymers[8–10] can also show good behavior, but the properties of the interface between the polymer and the organic semiconductor can be complex and difficult to understand. In addition, lithographic techniques that are capable of patterning polymer electrodes in transistors with submicron or nanoscale channel lengths are still under development. Devices that use metal electrodes evaporated on top of a semiconductor film (i.e., top contacts) represent one of the most commonly used designs. Devices of this type often show good characteristics, but the standard patterning technique (i.e., shadow masking) is not capable of high resolution, and the chemical fragility of most organic semiconductors precludes the use of photolithography, electron beam lithography, or other established approaches. In addition, the interface between the evaporated metal and the semiconductor in these types of top contact devices can be diffuse on a nanometer scale; the degree of metal penetration into the semiconductor can be difficult to control.

Our recent work demonstrated that many of these difficulties can be avoided by using soft contact lamination

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procedures.[11,12] In this approach, source/drain electrodes of a chemically inert metal such as gold are formed on an elastomeric substrate (polydimethylsiloxane PDMS) or on a thin film of PDMS cast against a rigid or flexible support. Bringing this element into conformal contact with a substrate that supports a gate electrode, dielectric, and semiconductor yields a top contact laminated transistor. In this process, van der Waals forces hold the electrodes in contact with the semiconductor, without the use of pressure, heat, or adhesives. High-performance top contact transistors are formed without disturbing the chemistry or the morphology of the underlying organic semiconductor. The use of high-resolution, gold-coated rubber stamps that provide a relief structure in the geometry of source/drain electrodes adds flexibility to this approach, since it eliminates the need for direct patterning of the electrodes. This stamp-based method provides a remarkably simple route to organic transistors with channel lengths deep into the nanometer regime.[5] It also provides electrodes with pristine, bare gold surfaces that have not been exposed to the various processing steps that would otherwise be required for their patterning. Our recent work introduced these techniques and demonstrated their use for building high-performance transistors and simple circuits.[5,11,12] It also outlined some practical benefits for circuit and device applications. To apply this method to basic study of charge transport in nanoscale transistors and to improve further the behavior of the laminated contacts, it is necessary to distinguish between intrinsic device properties and those that are dictated by the electrical interface between the metal and semiconductor.

This article presents a systematic and detailed study of the electrical properties of contacts formed by laminating stamp-based gold electrodes against the organic semiconductors pentacene and copper hexadecafluorophthalocyanine (FCuPc) in transistors with channel lengths between 5 and 50 μm and channel widths between 50 and 400 μm. It also compares the results to those obtained from devices that use conventional top contact gold electrodes formed by electron beam evaporation through a shadow mask. The contact resistance calculations follow empirical models that were first applied to amorphous silicon thin film transistors with top contact geometries by Luan and Neudeck[13] and Kanicki *et al.*[14] This analysis is valid for devices that have ohmic contacts and that use semiconductors with mobilities that are independent of gate voltage. The procedures use channel length dependent current/voltage characteristics to determine a gate voltage dependent contact — or parasitic — resistance. Related models have recently been applied to extract the contact resistance between bottom contact polymer electrodes and polymer semiconductors[8,9] and of top contact evaporated gold electrodes on pentacene[15] and oligothiophenes.[16]

II. DEVICE STRUCTURES AND CHARACTERIZATION

Figure 1(a) schematically illustrates the procedures for assembling laminated, stamp-based transistors. High-resolution rubber stamps [polydimethylsiloxane (PDMS), Sylgard 184, DowCorning] were made by casting and curing against photolithographically defined masters that consist of patterned photoresist (SU-8-5, Microchem Corp.; thickness approximately 7 μm) on silicon substrates. Briefly (2–5 s) exposing the stamps to an oxygen plasma forms hydroxyl groups on the surface. Electron beam deposition of Ti (1 nm, 0.3 nm/s) followed by Au (15 nm, 1 nm/s) with a metal flux perpendicular to the stamp surface leads to deposition predominantly on the raised and recessed regions of the stamp and not on the sidewalls. In this way, electrically isolated thin metal electrodes with the geometry of the relief structure [i.e., source/drain electrodes with given channel width (W) and channel length (L)] are formed.

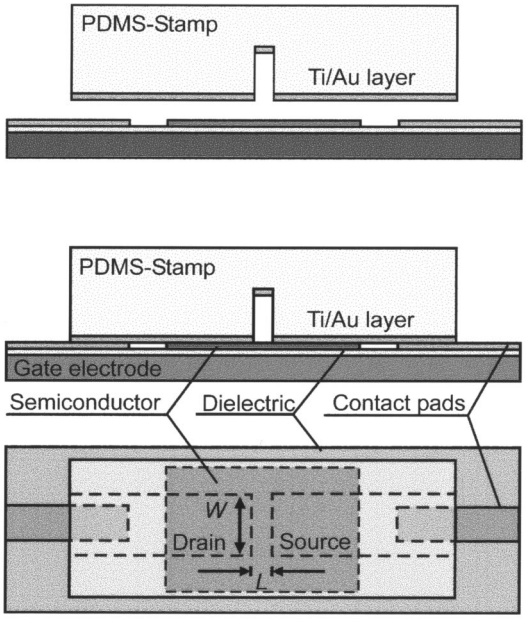

FIG. 1. Schematic illustration of a thin film transistor built by soft contact lamination of a metal-coated rubber stamp. An elastomeric stamp (polydimethylsiloxane, PDMS) with features of relief in the geometry of source/drain electrodes is coated with 1 nm of Ti and 15 nm of Au by electron beam evaporation. A collimated metal flux ensures deposition of metal only at the raised and recessed regions but not on the sidewalls. Bringing this stamp into conformal contact with a substrate that supports a semiconductor, dielectric, and gate electrode produces a transistor whose channel width (W) and channel length (L) are defined by the geometry of the stamp relief.

Bringing such a metal-coated stamp into conformal contact with a smooth substrate that provides a gate electrode, a dielectric, and a thin organic semiconducting film leads to multiple independent electrical contacts and formation of a complete top contact organic thin film transistor. The ''wetting'' contact that establishes connection between the gold-coated stamp and the semiconductor typically forms spontaneously. It is mechanically robust (i.e., structures with the stamps in place could be turned upside down without losing contact), yet fully reversible Metal-coated stamps can be removed from the substrate after the measurements without any visible change of the semiconductor. Although the microscopic physical nature of the contact has not yet been fully determined, measurements on the laminated transistors described here provide detailed information on its good electrical characteristics.

A highly doped silicon wafer provides a common gate electrode for these devices; a uniform 300 nm thick layer of

thermally grown SiO_2 (Process Specialties Inc.,) on this wafer serves as a gate dielectric. Thin films (25 nm) of copper hexadecafluorophthalocyanine (FCuPc, Aldrich, sublimated, deposition at 0.1 nm/s at 120 °C substrate temperature) and pentacene (Aldrich, deposition at 0.06 nm/s at room temperature) were thermally evaporated through a shadow mask with 3 mm×4 mm rectangular openings. Trilayers of Ti(1 nm)/Au(40 nm)/Ti(10 nm) deposited onto the silicon substrate through a shadow mask provide probing pads that connect to the raised regions of the stamp. The transistors were measured using a standard semiconductor parameter analyzer (HP 4155).

We used stamps with different source/drain electrode dimensions to extract the parasitic resistance associated with the laminated contacts. Each stamp supported several arrays of independent devices of either constant channel width (200 and 400 μm) or constant W/L ratio (10 and 20). The channel length varied from 50 to 5 μm. For comparison, we used the same substrates as for the stamp-based devices, but with conventional top gold source/drain electrodes (50 nm, 1 nm/s) evaporated directly onto the pentacene through a shadow mask. The channel width of these transistors was 2.5 mm and the channel length varied from 75 to 500 μm. Channel lengths below 75 μm were difficult to produce reliably by shadow masking.

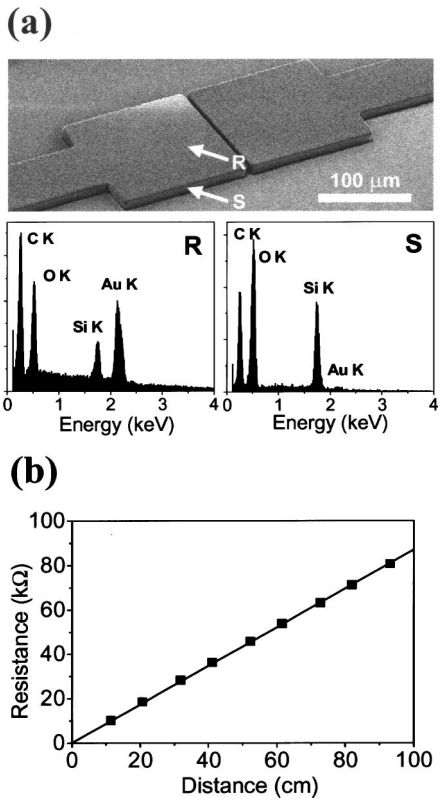

FIG. 2. (a) presents a scanning electron micrograph of an angled view of a metal-coated rubber stamp with relief in the geometry of transistor source and drain electrodes. In this case, the width and length of the channel are ~100 and 2.5 μm, respectively. The x-ray spectra indicate that the metal bilayer coating of Ti (1 nm) / Au (15 nm) exists on the raised and recessed portions (R) of the stamp, but not on the sidewalls (S). (b) shows the measured resistance as a function of length of a serpentine resistivity test structure formed with a Ti/Au-coated stamp that has relief in the geometry of a line that is 45 μm wide and 90 cm long. The slope of the linear increase of resistance with wire length yields a resistivity of $5.8\cdot10^{-6}\ \Omega$ cm.

III. RESULTS AND DISCUSSION

The absence of electrically continuous metal films on the sidewalls of relief on the stamps is crucial to the proper operation of these structures. Figure 2(a) shows an angled view of a coated stamp that exhibits the necessary vertical or slightly re-entrant sidewalls. The x-ray emission spectrum of a typical spot excited with a focused electron beam [JEOL JSM-5600LV equipped with an energy dispersive x-ray analysis spectrometer] on a raised/recessed region of this stamp is shown in the bottom left frame of Fig. 2(a). The right frame shows a similar spectrum collected from the sidewall, which indicates very little if any gold. To verify further that the stamps do not have significant amounts of metal on the sidewalls, and to illustrate that they have the expected electrical properties, we built stamps with relief in the geometry of a 45 μm wide and 90 cm long serpentine line with ten connecting probe pads. Coating such a stamp with Ti (1 nm)/Au (15 nm) using the previously described procedures and placing it on a glass slide with matching evaporated probe pads (Ti/Au/Ti) forms a resistivity test structure. Figure 2(b) shows results from measurements on such a structure. The slope of the linear increase of resistance with wire length yields a resistivity of $5.8\cdot10^{-6}\ \Omega$ cm, which is sufficiently small for our transistor measurements described below. This value is also comparable to measurements on similar thin films deposited on rigid substrates. The results indicate that there is no significant conduction from the raised to the recessed regions of the stamp. They also suggest that the possible presence of nanocracks (unobservable directly using optical or scanning electron microscopy) in the gold films on the rubber stamps do not affect significantly the electrical properties of laminated electrode structures with dimensions in the range of a few to tens of microns.

In order to determine certain elementary aspects of the laminated contacts, we examined first the current/voltage characteristics of devices built with both *n*- and *p*-channel organic semiconductors. Figure 3 presents measurements from a typical FCuPc (*n*-channel)[17] transistor with stamp-based laminated electrodes. This device has a channel width and length of 400 and 8 μm, respectively. The source-drain current (I_{SD}) saturates in the expected way, as shown in Fig. 3(a). The response at source-drain voltages that are much lower than the gate voltage (i.e., the linear region of a well-behaved transistor) shows highly linear behavior, which is consistant with ohmic contacts between the semiconductor and the laminated gold electrodes [Fig. 3(b)]. Similar behavior is observed with *p*-channel pentacene transistors, as illustrated in Fig. 4. For this device, the channel width and length are 400 and 20 μm, respectively. For both semiconductors, the transistors show on/off ratios of 10^3-10^5 (relative to a gate voltage of 0 V) that are comparable to those observed in devices built with these materials in the more established ways (i.e., with microcontact printing, shadow masking, etc.). The gate leakage of these devices is below 5 nA at

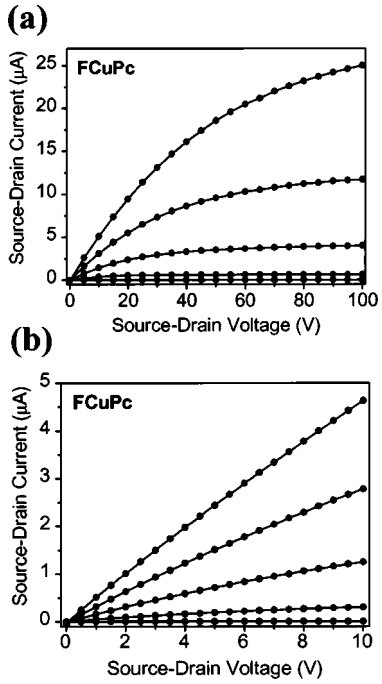

FIG. 3. (a) shows current-voltage characteristics of an organic thin film transistor made by soft contact lamination of a metal-coated stamp. The semiconductor is a thermally evaporated film (thickness ~25 nm) of FCuPc (copper hexadecafluorophthalocyanine) on a highly doped silicon wafer that serves as a common gate electrode. A uniform 300 nm SiO_2 layer provides a gate dielectric. The channel width is 400 μm, the channel length is 8 μm. The gate voltage varies between 0 and 100 V in steps of 20 V. The on/off ratio is $\sim 10^4$. (b) shows the response at small source-drain voltages. The linear current-voltage characteristics when the source-drain voltage is much smaller than the gate voltage suggest ideal ohmic contacts between the laminated electrodes and active region of the transistor channel.

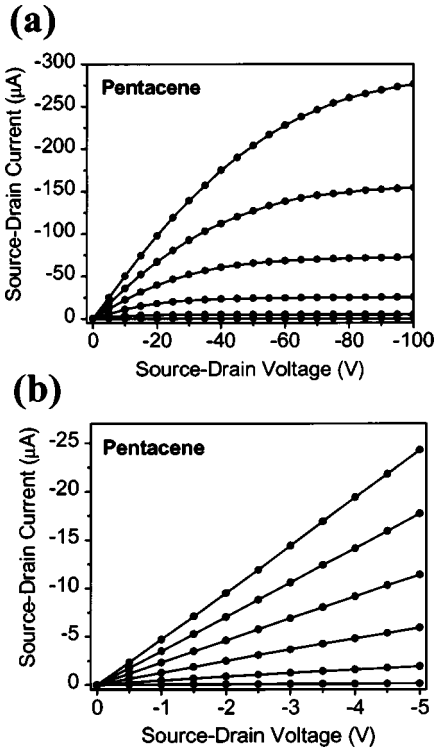

FIG. 4. (a) shows current-voltage characteristics of a laminated transistor with a thermally evaporated film (thickness ~25 nm) of pentacene as the semiconductor. The channel width is 400 μm, the channel length is 20 μm. The gate voltage varies between 0 and -100 V in steps of -20 V. The on/off ratio is $\sim 10^4$. (b) shows the linear region of the curves in (a). The linear current-voltage behavior illustrated in (b) is consistent with ideal ohmic contacts between the laminated electrodes and the transistor channel.

maximum gate voltage. The floating gold film in the recessed regions of the stamp does not seem to affect the dc behavior of the laminated trasistors significantly. For further investigation of the laminated contacts we focused on pentacene owing to its high mobility, which emphasizes the effects of parasitic resistances associated with the contacts.

The effective mobility of an organic semiconductor in a transistor is typically calculated either in the regime where the source-drain current depends linearly on the source-drain voltage (linear regime) or where the source-drain current is independent of source-drain voltage (saturation regime).[18] In the saturation regime, the gradual channel approximation and the assumption that the field effect mobility is independent of the gate voltage yields the following expression for the saturation current $I_{DS,sat}$:

$$I_{DS,\mathrm{sat}}=\frac{W}{2L}\mu_{\mathrm{sat}}C_i(V_G-V_{T,\mathrm{sat}})^2, \tag{1}$$

where μ_{sat} is the effective mobility, $V_{T,\mathrm{sat}}$ is the effective threshold voltage, and C_i is the capacitance of the dielectric. Thus, the square root of the saturation current is linearly dependent on the gate bias. Figure 5(a) shows a plot of $(|I_{DS,\mathrm{sat}}|)^{1/2}$ at a source-drain voltage of -100 V versus gate voltage for the same pentacene transistor as in Fig. 4. The data exhibit linear behavior for gate voltages over -20 V. The slope and intercept of the linear fit yield an effective mobility of $\mu_{\mathrm{sat}}=0.32\pm0.02\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ and a threshold voltage of $V_{T,\mathrm{sat}}=-14.9\pm0.8$ V, for this particular device. (Unless otherwise specified, the error bars here and elsewhere correspond to experimental and fitting related uncertainties for measurements on a single device. Device–to–device variations are typically significantly larger than these error bars. Over the course of this study the average saturation mobility of the pentancene varied between 0.3 and 0.6 $\mathrm{cm^2\,V^{-1}\,S^{-1}}$. The average saturation regime threshold voltage fluctuated between 11 and 19 V. For one set of measured transitors on a small region of pentacene the absolute deviations of the saturation monility and the threshold voltage were $\pm0.04\ \mathrm{cm^2\,V^{-1}\,S^{-1}}$ and ±3 V, respectively.)

In the linear regime, Eq. (2) is valid

$$\frac{dI_{DS}}{dV_{DS}}=\frac{W}{L}\mu_{\mathrm{lin}}C_i(V_G-V_{T,\mathrm{lin}}). \tag{2}$$

Here, the slope and the intercept of the linear fit to the experimental data [Fig. 5(b)] determine the effective mobility and threshold voltage, respectively. For the same transistor as above we calculate an effective mobility of $\mu_{\mathrm{lin}}=0.26\pm0.01\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ and a threshold voltage of $V_{T,\mathrm{lin}}=-20\pm1$ V. It is clear from Figs. 4 and 5 that the standard linear and saturation regime analyses work well for laminated transistors and that the observed data agree with theory. We note

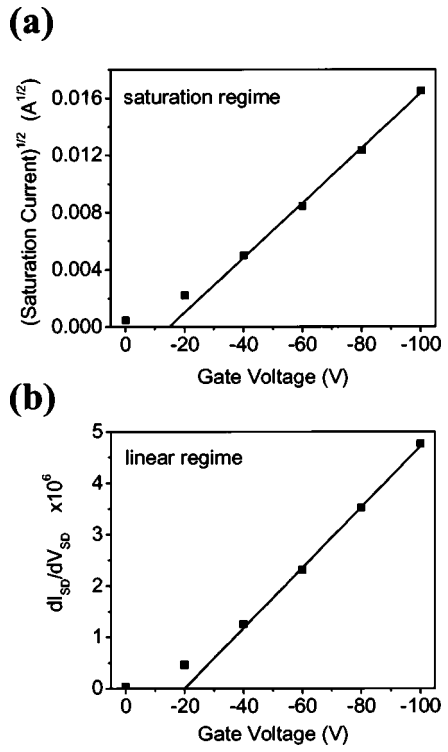

FIG. 5. (a) shows a plot of the square root of the saturation current (at $V_{DS}=-100$ V) as a function of gate voltage for the laminated pentacene transistor whose characteristics are shown in Fig. 4. The slope and the x-intercept of the line fit to the linear part of the graph yield a saturation mobility of 0.32 $cm^2\ V^{-1}\ s^{-1}$ and a threshold voltage of -14.9 V, respectively. (b) shows a plot of dI_{DS}/dV_{DS} as a function of gate voltage for $V_{DS} \ll V_G$ of the same device. Here the slope and the x-intercept of the line fit yield a mobility of 0.26 $cm^2\ V^{-1}\ s^{-1}$ and a threshold voltage of -20.0 V. (Error bars correspond to experimental and fitting related uncertainties for measurements on a single divice. Typical device-to-device variations are on the order of ± 0.04 $cm^2\ V^{-1}\ S^{-1}$.)

that the computed linear mobilities are always lower than the saturation mobilities, and that this difference grows as the channel length decreases.

To gain a better understanding of the contacts, we studied the channel length dependence of the effective linear and saturation mobilities. Figure 6 shows the steady decrease of both mobilities with decreasing channel length for a typical set of laminated devices with a constant channel width of 200 μm. The data show that the linear mobility depends much more strongly on the channel length than the saturation mobility. This result is not unexpected, since the linear regime is more strongly affected by interface properties and contacts than the saturation regime. Any voltage drop across the electrode/semiconductor interfaces will lower the effective voltage across the channel and, therefore, the currents that are used to compute the linear mobility. In the saturation regime, however, this same voltage drop has only a relatively small effect since the source-drain current is already independent of the source-drain voltage. We noticed that for short channel lengths, the source-drain current saturates at higher source-drain voltages than for longer channel lengths. This observation is consistent with the increased importance of parasitic resistances associated with the electrodes at short channel lengths. We did not, however, observe any systematic channel length dependence of the effective threshold voltages. This result might be due to device–to–device variations which can exceed the effect of the channel length if the resistances associated with the contacts are small.

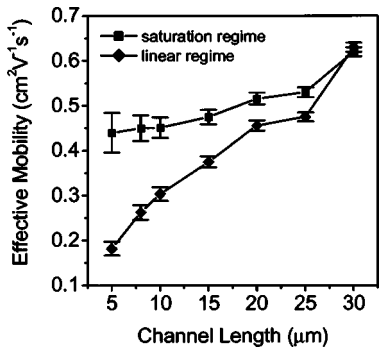

FIG. 6. Effective mobility in the saturation (solid squares) and linear (solid diamonds) regime as a function of channel length for a typical set of devices that use laminated source/drain electrodes on a single pentacene substrate. The channel lengths range from 5 to 30 μm; the channel width is 200 μm in all cases. Both mobilities decrease with decreasing channel length, which is consistent with non-negligible parasitic resistances associated with the contacts. This effect is more pronounced for the linear mobility than for the saturation mobility.

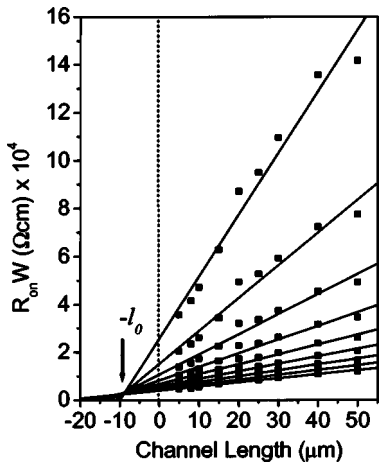

FIG. 7. Width normalized device resistance as a function of channel length at gate voltages from -20 to -100 V, extracted from transistors with channel lengths between 5 and 50 μm and a channel width of 400 μm on a single pentacene substrate. The y-intercepts of the fitted lines (solid lines) give the parasitic resistances at the various gate voltages. All fitted lines meet at a single point which defines a characteristic length, $l_0=9.7$ μm, and a characteristic normalized resistance, $(R_{on}W)_0=2$ kΩ cm.

The dependence of the current/voltage characteristics on channel length can be used to extract parasitic resistances that include various components related to the contacts and other effects that are independent of channel length. In the linear regime, the overall device resistance $R_{\rm on}$ can be written as the sum of the intrinsic channel resistance $R_{\rm ch}$ and a parasitic resistance R_p according to[13]

$$R_{\rm on}=\left.\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{V_{DS\to 0}}^{V_G}=R_{ch}+R_p=\frac{L}{W\mu_i C_i(V_G-V_{T,i})}+R_p, \tag{3}$$

where μ_i and $V_{T,i}$ are the intrinsic mobility and threshold voltage, respectively. The parasitic resistance R_p can be ex-

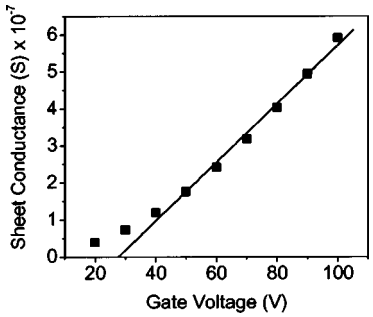

FIG. 8. Sheet conductance of the channel region as a function of gate voltage as derived from data in Fig. 7. The slope and *x*-intercept of the fitted line give an intrinsic mobility of 0.68 $cm^2\,V^{-1}\,s^{-1}$ and an intrinsic threshold voltage of 27.7 V, respectively.

tracted by determining R_{on} from the linear regime of the transistor characteristics and plotting the width-normalized $R_{on}\,W$ as a function of L for different gate voltages. Figure 7 presents such a plot for one representative set of devices with a channel width of 400 μm and channel lengths ranging from 5 to 50 μm. This plot contains various intrinsic and extrinsic device parameters that are extracted and discussed below.

According to Eq. (3), the slope of the $R_{on}\,W$ versus L plot contains the intrinsic mobility and threshold voltage of the channel, independent of the channel length. Thus, plotting the reciprocal slope, which is equivalent to the channel sheet conductance, versus the gate voltage should yield a straight line. Figure 8 shows the results. The slope and intercept of the linear least-squares fit determine an intrinsic mobility of $\mu_i = 0.68 \pm 0.03$ $cm^2\,V^{-1}\,s^{-1}$ and a threshold voltage of $V_{T,i} = -28 \pm 3$ V.

The parasitic resistance corresponds to the *y*-axis intercept of the extrapolated linear fit of R_{on} versus L. This resistance depends on the gate voltage as shown in Fig. 9. We analyzed several different sets of transistors with constant channel width (200 and 400 μm) or constant W/L ratio (10 and 20) as well as different pentacene film thicknesses (25, 10, and 3 nm) but no significant dependence on these parameters could be found. All devices showed a width-normalized contact resistance of 12 to 45 kΩ cm at a gate voltage of -20 V and 2 to 6 kΩ cm at -100 V. These values are comparable to those calculated by Luan and Neudeck for amorphous silicon transistors.[13] We note that the resistance of the laminated electrodes themselves is negligible. A laminated electrode of 15 nm Au, 400 μm wide, and 2 mm long gives a resistance of approximately 20 Ω, which is small compared to 50 kΩ that is the smallest parasitic resistance at -100 V for a 400 μm wide electrode. The parasitic resistance becomes significant compared to the device resistance at high-gate voltages even at channel lengths of 10 μm. This result highlights the importance of quantitatively understanding the contacts and of developing reproducible and reliable ways for forming them, especially for studies of nanoscale transport in devices with channel lengths in the submicron region.

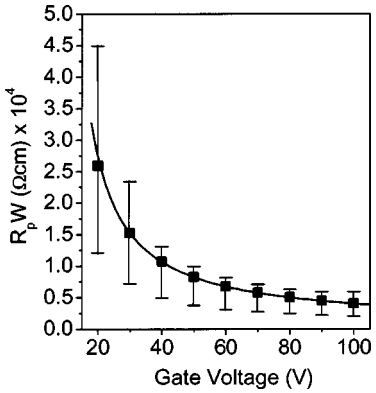

FIG. 9. Width normalized parasitic resistance as a function of gate voltage for devices summarized in Figs. 7 and 8. Fitting these data to the functional form given in the main text yields a contact mobility of 0.3 $cm^2\,V^{-1}\,s^{-1}$ and a contact threshold voltage of -8 V. The error bars indicate the entire range (i.e., maximum to minimum values) of width normalized parasitic resistances extracted from 16 different pentacene samples and 16 different transistor arrays with channel widths of 200 and 400 μm, channel lengths from 5 to 50 μm as well as a range of device geometries with constant W/L ratios of 10 and 20.

Since all linear fits through the $R_{on}\,W$ versus L data cross at a single point of $L = -l_0 = -9.7$ μm and $R_pW = (R_pW)_0 = 2$ kΩ cm, we can apply an empirical model for the parasitic resistance which was developed by Luan and Neudeck[13] for amorphous silicon top contact transistors. This model regards the parasitic resistance as a minimum effective contact resistance $(R_pW)_0$ in series with an accumulation channel of length l_0 under the source/drain electrodes

$$R_pW = \frac{l_0}{\mu_c C_i (V_G - V_{T,c})} + (R_pW)_0 . \tag{4}$$

Fitting the R_pW versus V_G plot to Eq. (4) yields a mobility of $\mu_c = 0.3 \pm 0.1$ $cm^2\,V^{-1}\,s^{-1}$ and threshold voltage of $V_{T,c} = -8 \pm 2$ V for the contact region. The empirical picture according to Eqs. (3) and (4) of a transistor with physical channel length L, includes an effective increased channel length of l_0 with an associated reduced mobility μ_c, and a series resistance of R_p. The lower mobility for the contact region (compared to the saturation, intrinsic, or linear mobilities) might not be unreasonable since the pentacene surface is exposed to light and air during sample preparation, which may lead to some degree of degradation and impurities at the interface between the contacts and the top surface of the pentacene. Also, current must flow from the electrodes and through the semiconductor to reach the active channel region. It is notable not only that the empirical models developed for the amorphous silicon devices describe the laminated pentacene devices well, but also that the values of the parasitic and gate independent contact resistances are similar. These observations provide additional evidence that the laminated contacts provide remarkably good electrical coupling to the organic semiconductor.

In order to compare the stamp based transistors with conventional evaporated top contact devices, we extracted the parasitic resistance of evaporated contacts in the same way as described above from devices of 2.5 mm channel width and 75 to 500 μm channel length. Figure 10 shows the results of laminated contacts as well as evaporated contacts as a function of gate voltage. The parasitic resistance of the latter is more than an order of magnitude higher than that of the former. The qualitive result is also observed for stamp-

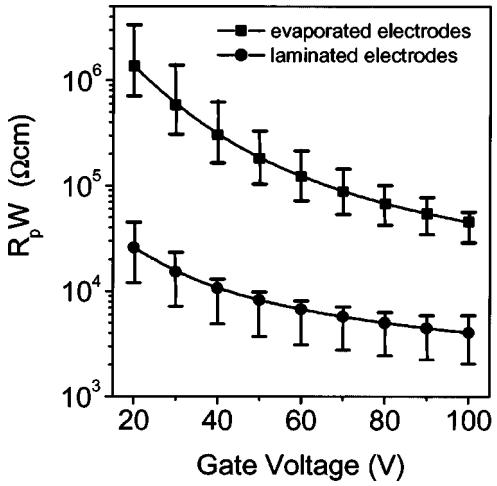

FIG. 10. Width normalized parasitic resistance as a function of gate voltage for laminated (same devices as in Fig. 9; solid circles) and evaporated (solid squares) gold source/drain electrodes. The values for the evaporated electrodes were extracted from analysis of devices with channel lengths between 75 and 500 μm and a fixed channel width of 2.5 mm. The evaporated devices show parasitic resistances that are more than an order of magnitude higher than those for the laminated devices. Error bars indicate the entire range (i.e., maximum to minimum values) of width-normalized contact resistances for all measured device sets.

based devices that have electrode dimensions comparable to those in the evaporated devices. This result explains, in part, the lower effective mobility and higher threshold voltages in evaporated devices compared to those of laminated devices that we observed in a previous study.[5] We also note that the evaporated devices showed less consistent performance compared to those built by lamination. Their properties were also sensitive to the evaporation rate. The results shown in Fig. 10 represent the range of contact resistances, obtained with an evaporation rate of 1 nm/s. The contact resistances increase with decreasing evaporation rates below 1 nm/s. Photoelectron spectroscopy studies by Watins, Yan, and Gao[19] and Shen and Kahn[20] found higher-charge injection barriers for electrons and holes in FCuPc and pentacene, respectively, for gold contacts formed by slow evaporation on top of the semiconductors than for those formed by deposition of the semiconductors on top of the gold. These results were explained by doping effects at the interface. The high contact resistances that we observed could also be caused by thermal or morphological degradation of the pentacene due to radiation, heat, or indiffusion of gold atoms into the organic. More detailed studies of the evaporated gold on pentacene interface will be necessary to explain these results fully.

IV. CONCLUSIONS

This article presents detailed measurements of several characteristics of top contact organic transistors formed by soft contact lamination. In *p*- and *n*-channel devices with pentacene and FCuPc as the semiconductors, respectively, the laminated source/drain contacts were found to have ohmic behavior; other device characteristics (i.e., effective mobilities, on/off ratios) were in the same range as those in devices built using other approaches with these materials. Additional measurements on large numbers of laminated devices with a range of channel lengths and widths show that, for channel lengths of less than 30 μm, the linear mobility decreases with decreasing channel length whereas the saturation mobility is only slightly reduced. Analysis of systematic measurements of the characteristics of transistors with different channel lengths reveals that the parasitic resistances associated with the laminated contacts depend on gate voltage in a manner that is remarkably consistent with the behavior of amorphous silicon top contact devices. In comparison, our measurements and analysis of evaporated gold contacts reveals much higher parasitic resistances than those in laminated devices. As a result, lower apparent mobilities are observed in the evaporated transistors than in the laminated ones, especially for relatively short channel lengths. The physical and possibly chemical differences between the contacts, which lead to these different electrical characteristics, are the subject of current study. Even in the laminated devices, the parasitic resistances begin to affect significantly the linear regime device performance at high gate voltages for channel lengths shorter than 10 μm. This effect will be important for circuit applications that rely critically on this linear response region. We note, however, that certain types of displays, such as electronic paper that uses microencapsulated electrophoretic inks, rely mainly on the saturation behavior of the transistors for the active matrix backplane.[7] In these systems, parasitic resistances at the contacts have a relatively small impact on the performance.

Methods for reducing the parasitic resistances clearly represent an important direction for engineering research in this field. They will also be important for charge transport studies in submicron or nanoscale transistors. Laminated electrodes are remarkably well suited for various chemical strategies for modifying the electrical properties of the interface that forms upon contact with an organic semiconductor. Through clever use of monolayer chemistry, it may be possible to reduce significantly the parasitic resistances in laminated devices, to levels below the values that we report here.

ACKNOWLEDGMENTS

The authors thank Zhenan Bao for help with purification and deposition of the FCuPc semiconductor and Julia Hsu for a careful reading of the manuscript. J. Zaumseil thanks the Dr.-Jürgen-Ulderup Foundation for financial support.

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