ADVANCED MATERIALS

High-Performance Contacts in Plastic Transistors and Logic Gates That Use Printed Electrodes of DNNSA-PANI Doped with Single-Walled Carbon Nanotubes**

By *Michael Lefenfeld*, *Graciela Blanchet*, and *John A. Rogers**

The field of plastic electronics has the potential to enable useful devices, such as flexible paper-like displays, woven electrotextiles, low-cost identification tags, etc., which might be difficult to achieve with conventional inorganic materials and processing technologies. Progress in this area is driven partly by the development of high-speed printing approaches and associated materials that can be used to pattern circuits over large areas at low cost. Several techniques have been explored, including the photochemical conversion of polymers from non-conducting to conducting states,[1] specialized adaptations of ink jet[2] and screen printing,[3,4] certain types of molding[5,6] and imprinting[7] approaches, and a nanotransfer printing method.[8,9] Microcontact printing[10] has been shown to be useful for patterning gold and silver source/drain electrodes and interconnects in large-area flexible circuits for paper-like displays and other devices.[11,12] We recently reported a purely additive thermal transfer printing technique that is capable of directly patterning multiple layers of organic electronic materials with micrometer (~5 μm) resolution over large areas (well over 3 m^2) and with multilevel registration (maximum misregistration of <200 μm over the entire >3 m^2 printed area).[13] In this approach, conducting polymers are transfer printed, layer by layer, from donor sheets onto a circuit substrate using localized laser-induced heating. This method has a completely dry, solventless operation that avoids many of the problems associated with chemical incompatibilities that commonly arise in solution-processed multilayer plastic circuits. For many envisioned applications in large area displays and other systems, the circuits are simple enough that registration errors and multilevel stack integrity are not limiting. In addition, for these applications the ability to print lines with better than ~25 μm resolution rapidly and over large areas begins to enable circuits that could have some commercially significant applications even with existing organic semiconductors. The performance, of course, benefits not only from high-resolution printed electrodes (i.e., short transistor channel lengths), but it also relies critically on low resistance coupling of the electrodes to the semiconductor layers. (It also depends, of course, on good dielectrics,[14] semiconductors, and other factors that are not the focus of this manuscript.) This paper examines the remarkably good contacts that form when pentacene and copper hexadecafluorophthalocyanine (FCuPc) are deposited onto printed dinonylnaphthalene sulfonic acid doped polyaniline/ single-walled carbon nanotube (DNNSA-PANI/SWNT) electrodes to produce n- and p-type transistors and complementary inverter circuits. The transistors that we examine have a range of channel lengths, as small as 15 μm, which can be formed reliably with this printing technique (channels as short as 5 μm are possible, with lower yields). The low resistance contacts and the ability to print the electrodes with high resolution are both important features of this system.

The devices use flexible poly(ethylene terephthalate) (PET; 175 μm thick) substrates, indium tin oxide (ITO; 100 nm thick) gates, and rod cast gate dielectrics of an organosilsesquioxane glass resin[14] (GR; ~2 μm thick). A thermal laser printer induces localized transfer of a thin layer of DNNSA-PANI/SWNT from a donor sheet that is pressed against the GR/ITO/PET substrate. The Experimental section provides some details. Figure 1a,b presents micrographs of patterns formed in this way. The roughness on the edges of the lines is <5 μm, which is comparable to the spot size of the laser beam that induces transfer. The electrodes are ~1 μm thick, and they have a conductivity of ~3 S cm.[13] For many types of non-emissive displays (e.g., liquid crystal or electrophoretic systems), the modest conductivity of the doped material is acceptable. There are, however, significant benefits to improving its conductivity and/or combining it in a circuit with other materials that are better conductors. These directions are the focus of current work. The SWNT doping approach provides a ~10^4 increase in the conductivity compared to DNNSA-PANI. As the scanning electron microscopy (SEM) image in Figure 1b indicates, the SWNTs in the DNNSA-PANI matrix are pulled out at the edges during the printing, where they couple directly to the semiconductor in the channel region. The printer itself supports overlay accuracies that can be as good as ~10 μm. Routinely achievable accuracies are ~200 μm, limited only by the relatively simple manual procedures that we currently use for inserting the substrate into the printer.

The transistors are completed by thermally evaporating thin (~25 nm thick) layers of organic semiconductors on top of the printed structures through a shadow mask. The resulting bottom contact (i.e., source/drain electrodes beneath the semiconductor) geometry enables the organic semiconductor, which is often the most chemically and mechanically fragile material in a plastic circuit, to be deposited last, after all of the other layers have been formed. It also places the bottom edge of the electrodes immediately adjacent to the accumulation layer that develops at the semiconductor/dielectric interface when a gate voltage is applied. With most materials and

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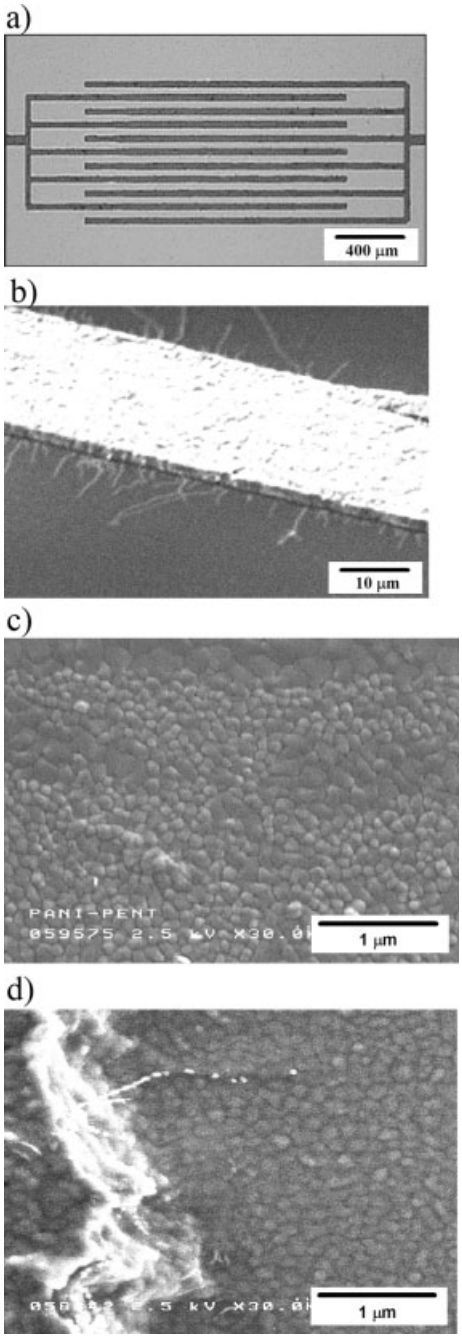

Fig. 1. Micrographs of thermal transfer printed patterns of DNNSA-PANI/SWNT and transistors that use them for source/drain electrodes. a) Optical micrograph of interdigitated source/drain electrodes for an n-channel transistor in a complementary inverter circuit. b) Scanning electron microscopy (SEM) image of a printed DNNSA-PANI/SWNT line. The edge roughness is < 5 μm, which is comparable to the size of the laser spot used to induce transfer. SWNTs are pulled out of the PANI matrix at the edges during printing; they appear as bright lines in the image shown in (b). c) SEM image of a region in the middle of the channel of a pentacene transistor that uses printed DNNSA-PANI/SWNT electrodes like those shown in (a) and (b). The grains in the polycrystalline pentacene film are clearly visible. d) SEM image of a region next to the source electrode (left side) of the transistor. These SEM images illustrate that the grain size and morphology of the film are uniform throughout the channel.

patterning techniques, however, this bottom contact geometry can suffer from contacts that are either non-ohmic or highly resistive compared to source/drain electrodes deposited on top of the semiconductor (i.e., top contact geometry).[15–18] These effects can be significant even for devices with channel lengths of several tens of micrometers. The poor contacts, which have been attributed partly to disturbed semiconductor crystal growth near the electrodes can in some cases be improved by carefully controlling the processing conditions[12] or by chemically treating the electrodes.[15,19] The DNNSA-PANI/SWNT system leads naturally to complete uniformity in the grain size and morphology of pentacene films across the electrode and entire transistor channel (see the SEM images in Fig. 1c,d). Furthermore, these bottom contact devices show remarkably good performance. Both of these results are unusual; they are not typically observed in pentacene devices with conventional bottom contact bare metal source/drain electrodes. Figure 2 shows the characteristics of pentacene and FCuPc transistors that use electrode patterns similar to those shown in Figure 1. The inset in Figure 2a and the dotted line in Figure 2b illustrate the linear current–voltage characteristics at source/drain voltages (V_{SD}) that are smaller than the gate voltage (V_G). This behavior is consistent with ideal ohmic contacts (or non-ohmic contacts that have negligibly small effects).

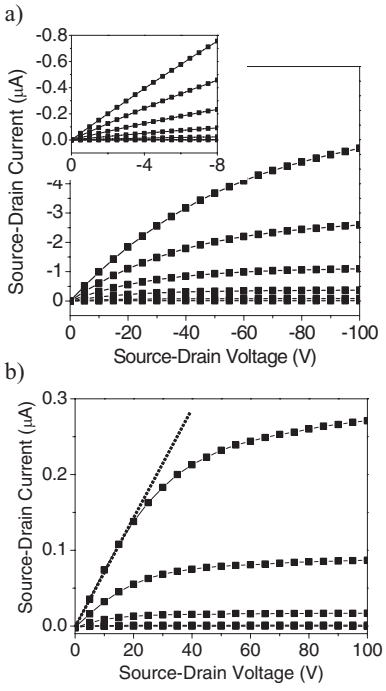

Fig. 2. Current–voltage characteristics of organic transistors that use thermal transfer printed DNNSA-PANI/SWNT source/drain electrodes, ITO gates, glass resin gate dielectrics, and plastic substrates. a) p-Channel transistor that uses a thin (25 nm) film of pentacene deposited onto the electrodes. The gate voltage varies from 0 to –100 V in steps of –20 V. The channel length and width are 15 μm and 0.5 mm, respectively. The inset shows the linear behavior of the device at small source–drain voltages. b) n-Channel transistor that uses a thin (25 nm) film of copper hexadecafluorophthalocyanine. The gate voltage varies from 0 to 100 V in steps of 20 V. The channel length and width are 50 μm and 2.5 mm, respectively. This transistor also exhibits linear behavior, as indicated by the dashed line. The characteristics of these devices are consistent with contacts that have ideal ohmic character (or negligible influence on the performance).

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Effective mobilities of these devices and similar ones with different channel lengths (L) are comparable to (for FCuPc) and larger than (by a factor of ~1.5, for pentacene) those of similar devices that use top contact evaporated gold (50 nm thick; deposited at 1 nm s^{-1}) source/drain electrodes and the same channel geometries. To understand these results, and to quantify further the behavior of the contacts, we studied the channel length dependence of the device resistance at small source/drain voltages in pentacene transistors, where the effects of contacts should be most pronounced, due to the relatively high mobility of this organic semiconductor. (The low mobility of the FCuPc frustrates a similar analysis of contacts in the n-type devices. In those cases, the effects of contacts are small compared to the channel resistance for the entire range of channel lengths that can be achieved with our printing technique.) In this regime, the "on" resistance, R_{on}, can be related to an L-dependent channel resistance, R_{ch}, and an L-independent parasitic resistance, R_p, that is associated with the contacts, according to models developed for amorphous silicon top contact transistors[20]

$$R_{on} = \left.\frac{\partial V_{SD}}{\partial I_{SD}}\right|_{V_{SD}\to 0}^{V_G} = R_{ch} + R_p = \frac{L}{W\mu_i C_i\left(V_G - V_{T,i}\right)} + R_p \quad (1)$$

where W is the channel width, C_i is the capacitance of the gate dielectric, I_{DS} is the source/drain current, μ_i is the intrinsic mobility, and $V_{T,i}$ is the intrinsic threshold voltage. Figure 3 shows a plot of R_{on} as a function of L at various gate voltages. The y-intercepts of the line-fits to data collected at each V_G determine R_p. The results show that R_pW is of the order of ~0.1 MΩ cm or less (the precise value is near our experimental limit, which is defined mainly by device-to-device variations due to micrometer-scale roughness on the edges of the printed electrodes and to slight spatial non-uniformities in the properties of the dielectric and semiconductor layers). These small parasitic resistances explain, in part, the improved performance of pentacene transistors that use printed DNNSA-PANI/SWNT compared to those that use evaporated top contact gold electrodes.[17,18] In the case of FCuPc, it is likely that the relatively low intrinsic mobility (and resulting large R_{ch}) masks contact differences in these two cases, which leads to transistors with similar performance. Figure 3b shows a plot of the channel sheet conductance as a function of gate voltage, as computed from the slopes of the lines in Figure 3a. The linear fit determines μ_i and $V_{T,i}$ from the slope and x-intercept, respectively. It is notable that the linear ($\mu_{lin} = 0.20 \pm 0.03$ cm^2/V s), saturation ($\mu_{sat} = 0.20 \pm 0.02$ cm^2/V s), and intrinsic ($\mu_i = 0.24 \pm 0.03$ cm^2/V s) mobilities computed from the pentacene devices all yield similar results, to within experimental and fitting uncertainties. A slight decrease in the linear mobility with decreasing channel length is consistent with some small, but non-negligible, parasitic resistance. The on/off ratios in all of the devices are in the range of 10^5.

The ability to form high-performance n- and p-channel transistors with DNNSA-PANI/SWNT electrodes enables

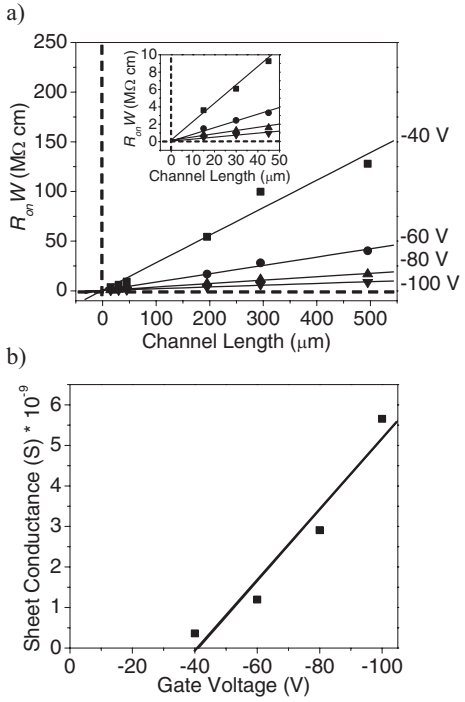

Fig. 3. Analysis of contact resistances and intrinsic channel mobilities from pentacene transistors with DNNSA-PANI/SWNT source/drain electrodes printed via thermal transfer. a) Width-normalized channel resistance (R_{on}) as a function of channel length at various gate voltages from –40 to –100 V. The inset shows line fits through data from devices with channel lengths less than 50 μm. The nearly zero y-intercepts of these lines indicate that the parasitic resistances associated with the contacts are small compared to the channel resistances for this range of channel lengths. The transistor width in all cases is 0.5 mm. (Data for the channel lengths longer than 50 μm were not used in the analysis.) b) Transistor channel sheet conductances, computed from the slopes of the fitted lines in (a), as a function of gate voltage. The slope and x-intercept of the line fit to these data define the intrinsic mobility and threshold voltage, respectively.

printed complementary inverter circuits, or logic gates. To illustrate this capability, we built arrays of inverters. The channel lengths and widths of the transistors were designed to match approximately the current outputs: the W/L values for the FCuPc and pentacene devices are 390 and 16, respectively, to compensate for the lower mobility of the FCuPc. The channel lengths, $L = 100$ μm, are the same in both cases. The n-channel transistor uses interdigitated electrodes like those shown in Figure 1a. These inverters use a common gate; their source/drain electrodes and the appropriate interconnecting lines are all printed in a single pass onto a substrate of glass resin/ITO/Mylar as described previously and in the Experimental section. The semiconductors are evaporated one after another onto the channel regions through metal shadow masks. The physical separation between the transistors is limited only by the resolution of the shadow masking and the overall size of each transistor. Figure 4 shows the transfer characteristics and the layout. These circuits exhibit gains greater than 10.

In summary, this communication reports on the excellent electrical properties of contacts in organic transistors and logic gates that use printed electrodes of DNNSA-PANI/SWNT in bottom contact configurations. The large grain sizes ob-

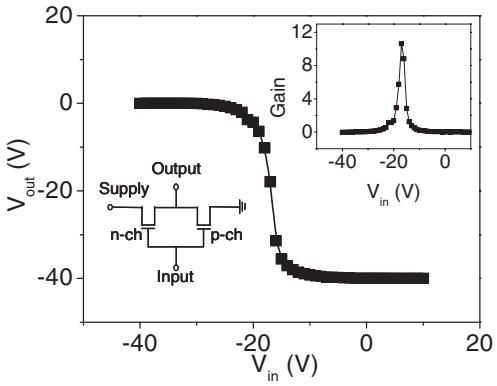

Fig. 4. Transfer characteristics of a complementary inverter circuit formed using n- and p-type organic transistors with DNNSA-PANI/SWNT electrodes printed via thermal transfer. The inset shows the layout of the inverter and the measured gain.

served at and near the contacts, which are identical in shape and size to those in the center of the channel, are consistent with these observations. The results provide some evidence to suggest that thermal printing with this class of doped conducting polymer or related materials might represent progress toward a useful strategy for building large-area circuits for realistic applications.

Experimental

The transistors and logic gates were fabricated on a 175 μm thick flexible poly(ethylene terephthalate) (PET) substrate with a 100 nm layer of indium tin oxide (ITO) as a gate electrode (commercially available from Southwall Technologies, Palo Alto, CA). The ITO layer was cleaned with a foam pad and a Liqui-Nox soap solution followed by a methanol rinse. A solution of an organosilsesquioxane (20 % solidsin propoxypropanol), GR-720F flake from Techneglas, dissolved in butanol was rod-cast onto the ITO surface to achieve an approximate thickness of 2 μm [14]. The resin was cured in an oven set at 130 °C for ~12 h. DNNSA-PANI/SWNT source and drain electrodes were thermal transfer printed from a 1 μm thick layer of this material cast on a PET backing and placed against the glass resin [13]. The printing apparatus uses a scanning 40 W 780 nm infrared diode laser that is split into 250 2 μm by 5 μm individually addressable spots [13]. Pentacene (CAS# 135-48-8) obtained from Aldrich was purified by vacuum sublimation immediately prior to deposition. Copper hexadecafluorophthalocyanine (FCuPc, CAS# 14916-87-1), also obtained from Aldrich, was purified by temperature-gradient sublimation in vacuum. Pentacene and FCuPc were then evaporated at pressures of ~10^{-7} torr onto the transistor channel region through a shadow mask at rates of 0.03 and 0.06 nm s^{-1}, respectively. For the FCuPc deposition, the transistor substrate was held at 75 °C. The pentacene was deposited onto substrates at room temperature. Electrical characterization was performed with an HP 4155 A semiconductor parameter analyzer. The dielectric capacitance was measured using an HP 4284 A precision LCR meter at a frequency of 1 kHz and a level of 1 V.

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A Miniaturized Enzyme Reactor Based on Hierarchically Shaped Porous Ceramic Microstruts**

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Heterogeneous enzymatic reactions such as ELISA-type immunoassays (ELISA: enzyme-linked immunosorbent assay) have recently been performed in microfluidic devices.[1,2] These miniaturized versions benefit from the larger surface-to-volume ratio of microchannel geometries and cost much less due to the small amounts of reagents necessary. At the same time, the separation of enzyme and product after the incubation step is ensured by immobilization of the enzyme, respectively the antibodies. Additional procedure steps like reagent preparation and detection of products have also been integrated to form so-called "labs-on-a-chip" or "micro-total-analysis systems" (μ-TAS).[3,4]

However, since liquid flow inside small channels is strictly laminar under almost any practical conditions,[5] the mixing of reactants, respectively the access of substrate molecules to the enzyme becomes more difficult. Mixing is diffusion limited in the absence of turbulent flow. Although it is possible to elon-

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