Large area, high resolution, dry printing of conducting polymers for organic electronics

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We show here that thermal imaging, a nonlithographic technique which enables printing multiple, successive layers via a dry additive process can be used in combination with tailored printable conductors in the fabrication of organic electronic devices. This method is capable of patterning a range of organic materials at high speed over large areas with micron size resolution and excellent electrical performance avoiding the solvent compatibility issues currently faced by alternative techniques. Such a dry, potentially reel-to-reel printing method may provide a practical route to realizing the expected benefits of plastics for electronics. We illustrate the viability of thermal imaging and imageable organics conductors by printing a functioning, large area (4000 cm^2) active matrix backplane display circuit containing several thousand transistors. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1533110]

Organic electronic systems offer the advantage of low weight, mechanical flexibility, and large area coverage at potentially lower cost. Although the fabrication of functioning plastic transistors using approaches such as ink jet, dye, transfer, lithography, and stamping has been described in the literature,[1–6] designing a set of chemically compatible materials that may ultimately allow for the sequential application of liquid layers, represents a major technical barrier. These material issues jeopardize the vision of printing inexpensive, throwaway plastic electronic components in a printing press and at high speeds. While the present set of materials are not suitable for printing thin film transistors (TFT) from sequential liquid layers neither can printing presses hold the resolution and registration required for device fabrication. In time, these difficulties may be surpassed and the vision of printing of organic electronics devices in a press may come to pass but that promise is, at minimum, a few years away.

It is perhaps more practical today to consider fabricating organic electronic devices with printing techniques that circumvent the serious materials and process issues presently associated with printing in a press. Thermal imaging,[7] a technique that enables the printing of multiple, successive layers, via a dry additive process provides an attractive alternative path. With printing proceeding via the ablative transfer of solid layers the solvent compatibility issues that are encountered when printing sequential layers from solution are entirely avoided. Over the last ten years DuPont has developed a platform of digital products based on thermal imaging, recently commercialized digital color proofing, developed digital color filters, and currently evaluating organic electronics. In all cases the design of the printable material set has been the key enabler.

Thermal imaging allows for the patterning of a range of organic materials at high speed, over large areas, and with micron size resolution. The imaging process, illustrated in

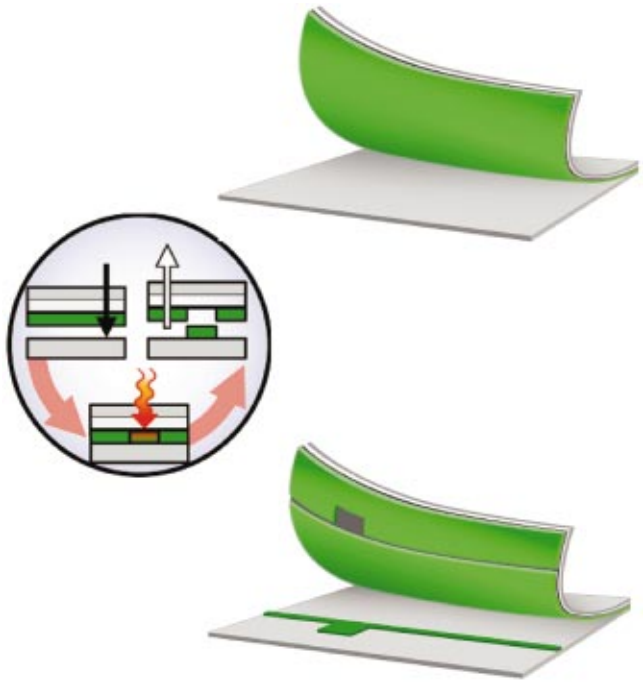

FIG. 1. (Color) *Illustration of the Printing Process*. The two flexible films, a multilayer donor and a receiver are held together by vacuum. The laser beam is focused onto a thin absorbing layer that converts light into heat, an optional ejection layer placed directly underneath, and a DNNSA–PANI/SWNT conducting layer coated on top. The heat generated at the metal interface decomposes the surrounding organics creating a gas bubble that when expanding propels the conducting layer onto the receiver. After imaging is completed the donor and receiver films are separated.

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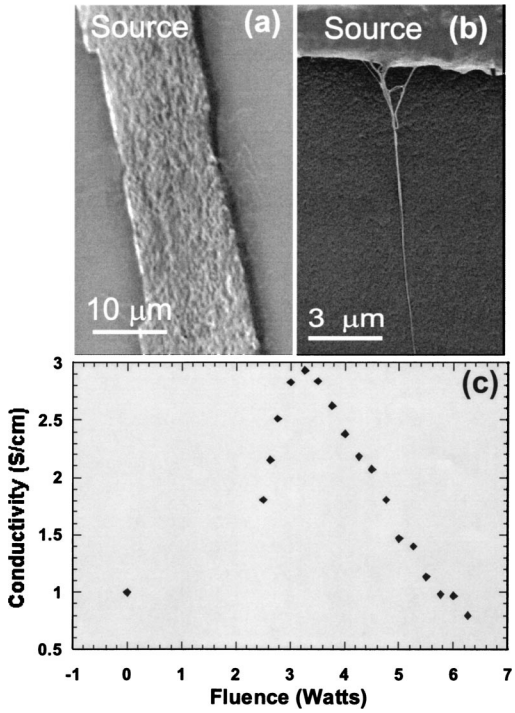

FIG. 2. *Morphology and conductivity of printed conducting sources*. The scanning electron microscopy on the upper left [2(a)] shows a transferred PANI/SWNT 20 μm line. Numerous SWNTs anchored onto the edge of the conducting line and extending into the channel are also visible. The micrograph on the upper right [2(b)] shows a single SWNT rope extending from the PANI/SWNT source line into the channel. The plot in the lower frame [2(c)] shows the conductivity, σ, of the printed line, in S/cm, as a function of transfer laser fluence, in W, is shown later.

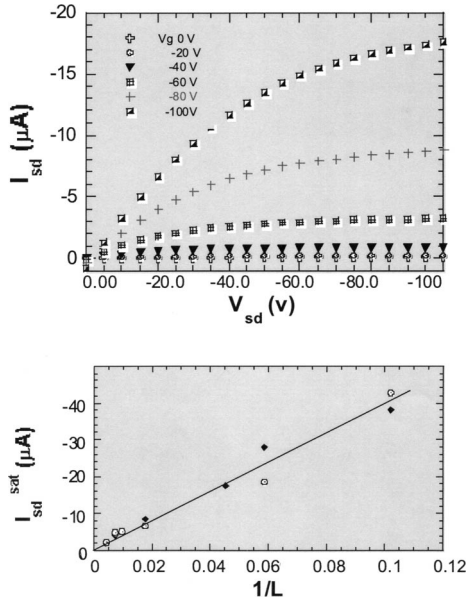

FIG. 3. *I–V characteristics of a printed* TFT. The *I–V* curves in the top graph correspond to a TFT comprising an ITO gate, a glass resin dielectric, printed PANI/SWNT source and drain (750 μm channel width and 22 μm channel length) and evaporated pentacene. The plot shows I_{sd} the source drain current as a function of V_{sd}, the source-drain voltage. The gate voltages, V_g, was varied from 0 to -100 V, in 20 V steps shown in the inset. The mobility was computed using the saturated I_{sd} as a function of V_g. The lower graph shows that the saturated I_{sd}, at $V_g = -100$ V scales inversely with L, the channel length, for neighboring transistor arrays. Transistors printed from the same array are indicated in the same color (red or black).

Fig. 1, involves the pixelized transfer of a thin solid layer, encompassing a digital image, from a donor film onto a flexible receiver. A detail view of the film structure is also shown in the figure. The film is imaged as follows. A 40 W 780 nm infrared diode laser, split into 250 2.7 μm$\times$5 μm individually addressable spots, is focused through the donor base at a thin metal layer. The efficient conversion of light to heat at this interface decomposes surrounding organics into gaseous products. Their expansion thus propels the top layer of the donor film onto the receiver. In Fig. 1, a gate pattern is printed by selectively transferring the individual 5 μm $\times$2.7 μm pixels comprising the image of the gate layer from the polyaniline (PANI)/single wall carbon nanotubes (SWNT) layer onto the receiver. The sequential transfer of images from different solid layers builds multilayer devices.

The first step towards applying thermal printing to the fabrication of an all-printed electronic device is the design an imageable organic conductor. Early experiments[8] show that conducting polymers typically used in organic electronics, [i.e., poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid PEDOT/PSS, dodecyl benzene sulfonic acid doped polyaniline (DBSA–PANI) and camphor sulfonic acid doped polyaniline] cannot withstand the heat generated during thermal imaging. In contrast, DNNSA–PANI, a polyaniline synthesized via emulsion polymerization and doped with dinonyl naphthalene sulfonic acid (DNNSA) can be thermally imaged without backbone deprotonation. The inherently low conductivity, 10^{-4} S/cm, of DNNSA–PANI was increased four orders of magnitude by dispersing low concentrations of SWNT into the polymer solution.[8] In the examples that follow we used as printable conductor 3% SWNT dispersed in DNNSA–PANI.

Figure 2(a) illustrates a 20 μm DNNSA–PANI/SWNT source line printed via thermal imaging. Individual pixels seen as discrete steps along the line edge. The micrograph also shows SWNT ropes anchored at the line edge and extending into the channel. The result suggests that pixels may carry ropes that extend beyond their volume. Then, portions of a rope lying outside the pixel being transferred become visibly exposed if the neighboring pixel is not transferred. Figure 2(b) shows a single SWNT rope well anchored onto the edge of a PANI/SWNT source line. Figure 2(c) shows that the conductivity of printed line is highly dependent on process parameters, specifically laser power. The conductivity increases from threshold at 2.5–3.5 W decreasing thereafter. The decrease in conductivity at higher fluences merely reflecting the deprotonation of the PANI backbone at elevated temperatures. Conductivity was measured using a standard four-probe method and line thickness using a profilometer.

The *I–V* characteristics of a printed transistor are shown in Fig. 3(a). The structure of the transistor was as follows. A 100 nm indium tin oxide (ITO) film sputtered onto a 7 m Mylar substrate was used as the gate. A glass resin,[3] spun onto the ITO to about 1.5 μm in thickness, insulated the gate from the printed DNNSA–PANI/SWNT source and drain. Unpurified pentacene was deposited on top via thermal evaporation. The channel width (W) and length (L) of the printed was 750 μm in and 22 μm, respectively. The gate voltage, V_g, was varied from 0 to -100 V in -20 V steps. Printed transistors yielded stable bottom contact devices with on/off ratios ($>$1000) compatible with spin-cast dielectrics.

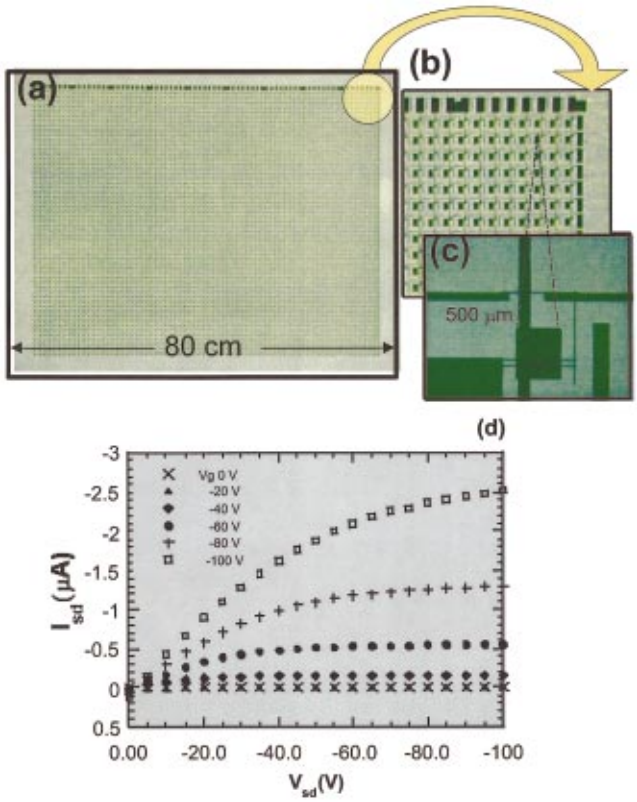

FIG. 4. (Color) *Printed* TFT *backplane*. A photograph of a 50 cm×75 cm printed panel is shown on the left [4(a)]. The micrograph at the top right [4(b)] shows a corner of the panel with 100 about TFT. The micrograph at the bottom right [4(c)] illustrates a single printed transistor. Figure 4(d) shows the $I-V$ characteristic of one of the transistors in the large printed panel. The gate voltage, V_g, varied from 0 to −100 V in 20 V steps, is specified on the right.

The effective mobility of the printed device was computed from the saturation current at high voltage was 0.3 $cm^2/V\,s$ while the mobility of a control device with Au source and drain and similar W/L was 0.15 $cm^2/V\,s$. Since SWNTs extending into the channel provide a larger surface area for the PANI to anchor the evaporated pentacene, better adhesion may also aid in a more efficient charge injection at the interface. Alternatively, the observed differences in mobility, i.e., contact resistance, may reflect differences in the charge injection mechanism at organic/organic and metal/organic interfaces.[9–12] Figure 3(c) shows the saturation current, I_{sd}, as a function of 1/L at maximum gate voltage (−100 V) for sets of transistors with 15 μm lines, 750 μm channel width, and channel lengths (L) ranging from 10 to 250 μm. As expected, the maximum ''on'' currents scales linearly with 1/L for a given array of transistors. The linear dependence extrapolating to zero reflects a relatively low contact resistance at the DNNSA–PANI/SWNT pentacene interface.

In addition, maintaining linearity even at small channel length suggests that the observed increase in mobility is not necessarily coupled to an effectively smaller channel at sites where metallic ropes extend into the channel. However, with such low density of ropes in the channel it is difficult to discount this possibility with certainty.

Figure 4(a) shows a picture of a TFT backplane, containing 5000 transistors with 20 μm channel printed onto a 50 cm×80 cm flexible substrate. The backplane has the same design as the circuit previously used for the electronic paper demonstration[3] and its electrical properties are also similar. An area containing about 100 TFTs is expanded in Fig. 4(b) and the micrograph of the single transistor in Fig. 4(c). The 3 S/cm gates were printed first by selectively transferring DNNSA–PANI/SWNT from a donor film onto a flexible receiver as previously described. The receiver was then removed for the lamination of a 1 μm methacrylate layer over the whole area and repositioned in registry for the printing of the source and drain layer. The backplane was completed by the evaporation of unpurified pentacene through a shadow mask. As seen in the micrograph, sources and drains are slightly shifted from the center of the gate. Although, the printing system maintains a one-pixel registration when imaging via the transfer of sequential layers onto a fixed receiver, it lacks built-in registration once the receiver is removed. Registration was achieved by aligning the receiver onto preset orthogonal edges on a carrier sheet that could, in turn, be precisely located onto the drum. This rudimentary approach maintained a maximum misregistration of less than 200 μm over the 4000 cm^2 area for any individual sample. The $I-V$ characteristics of the panel are shown in Fig. 4(d).

To conclude, the results presented here represent the demonstration that a the conducting layers of a functioning organic electronic devices can be printed, over large areas via the ablative, sequential transfer of solid films of conducting polymeric material. We illustrated the viability of thermal imaging and of the imageable conductors by printing a 50 cm×80 cm TFT backplane that is thin, of ultralow weight at a throughput of 1000 cm^2/min. In addition to the printing of the conductor we are currently developing materials and techniques for the printing of the gate dielectric and the semiconductor itself. Although the early results are quite promising, there remains a large amount of work before either the materials or the process are refined to adequate performance standards. Nevertheless, since thermal printing eliminates masking or photolithography also avoiding the need for interlayer solvents compatibility, the results presented here suggest that thermal imaging may bring organics electronics a step closer to reality.

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